

MODELING AND EXPERIMENTS WITH CARBON NANOTUBES FOR APPLICATIONS IN HIGH PERFORMANCE CIRCUITS

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1. SUMMARY

The work presented in this report is carried out under AFRL Grant No. FA9453-10-1-0002. The report is divided in following two parts: carbon nanotube (CNT) based electronics and graphene (G) based electronics. In Part I, CNT based electronics, electrical model of CNT-Field-Effect Transistor (CNT-FET) has been developed from the device physics for analysis and design of integrated circuits. The developed model is verified from published experimental data. Basic logic gates in complementary device structure such as inverter, negative and (NAND) and NOR gates have been designed. It is shown that voltage transfer characteristics are identical to corresponding complementary metal-oxide semiconductor (CMOS)-based logic. Very low-power CNT-FET based integrated circuits can be designed. Current CMOS technologies below 22nm nodes are plagued by the problems in copper interconnection due to its increased resistance and void formation. Exhaustive studies of single-wall CNT (SWCNT), multi-wall CNT (MWCNT) and bundle of single-wall CNT have been conducted for short, local and global interconnects and choice of suitability of their integration is suggested. Since CNT breaks down in integration with CMOS due to self-heating, an exhaustive study of self-heating effects in CNT has been conducted.

In Part II, graphene-based electronics, analytical current transport model of graphene nanoribbon (GNR) tunnel-FET (GNR-TFET) has been conducted extensively for integration with electronic design automation tools for design of graphene based integrated circuits. A BenchTop nano CVD-8G, (Chemical Vapor Deposition) System from Moorfield, Inc. UK has been purchased and installed for experimental characterization of atomic layer deposited graphene on different substrates for radiation-hardened studies.

2. INTRODUCTION

AFRL Contract No. FA9453-10-1-0002 was initially awarded from 07 December 2009 through 07 December 2013 (36 months) and further extended for another 36 months ending on 07 December 2016. The statement of the subject is broken into following five parts:

1. Modeling of single- and multi-walled carbon nanotubes and bundles of carbon nanotubes.
2. Current transport modeling of single-walled carbon nanotube field-effect transistors (CNT-FETs).
3. Electronic behavior modeling of carbon nanotubes and transistors to the molecular adsorbates for bio- and chemical sensing.
4. Exploratory research on current transport modeling in graphene, and experiments with the graphene material and characterization.
5. Radiation-hard graphene electronics.

2.1 Part I: Carbon Nanotube Based Electronics

Semiconductor Research Corporation (SRC) in its International Technology Roadmap of Semiconductors report (ITRS 2003) has referred to several non-classical devices, which could be the candidates of future technology to replace the existing silicon metal oxide semiconductor field effect transistor (MOSFETs) as the end of Moore's law approaches year 2020. Double gate MOSFET and FinFET are recognized as two of the most promising candidates for future very large scale integrated (VLSI) circuits. The CNT-FET is regarded as an important contending device to replace silicon transistors since many of the problems that silicon technology is facing are not present in CNTs. For example, carrier transport is one dimensional in carbon nanotubes; the strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration; and diameter is controlled by its chemistry and not by the standard conventional fabrication process.

For interconnects, as CMOS processes scale into the nanometer regime, lithography limitations, electromigration, and the increasing resistivity and delay of copper interconnects have driven the need to find alternative interconnect solutions. Carbon nanotubes have emerged as a potential candidate to supplement copper interconnects because of their ballistic transport and ability to carry large current densities in the absence of electromigration. Previous studies that assess the potential use of CNTs as interconnects primarily focus on the relative interconnect delay of CNTs to copper for sub-nm CMOS technology nodes. Carbon nanotubes are being explored extensively as the material for making future complementary devices, integrated circuits, interconnects and hybrid CMOS/nanoelectronic circuits.

In 1991, electron microscopist Sumio Iijima, of the NEC laboratories in Japan discovered the carbon nanotubes that are a tubular shape in the form of coaxial tubes of graphitic sheets, ranging from two shells to approximately fifty. These structures were categorized as MWCNTs. Subsequently growth of SWCNTs were reported.

Most SWCNTs have a diameter close to 1 nanometer, with a tube length that can be many thousands of times longer. The structure of a SWCNT can be conceptualized by wrapping an atomic thick layer of graphite called graphene into a seamless cylinder. Multi-walled carbon nanotubes consist of multiple layers of graphite rolled in to form a tubular shape. Since CNTs are planar graphite sheets wrapped into tubes, electrical characteristics vary with the tube diameter and the wrapping angle of graphene. One of the interesting features of the carbon nanotube is that it can be metallic or semiconducting with bandgap depending on its chirality. In the following, we discuss structure and electronic behavior of carbon nanotubes.

2.2 Structure of Carbon Nanotubes

There are four types of natural occurring carbon, diamond, graphite, ceraphite, and fullerenes. Fullerenes are molecules formed entirely of carbon and take the shape of a hollow sphere, ellipsoid, or a tube. Fullerenes that take the shape of a tube are called buckytubes or nanotubes.

Carbon nanotubes can be pictured as a result of folding graphene layers into a tubular structure as seen in figure 1. These cylindrical form of carbon nanotubes can be single-walled or multi-walled depending on the number of shells that form the tubular structure. Single-walled carbon nanotubes are composed of one shell of carbon atoms. Multi-walled carbon nanotubes have multiple nested shells of carbon atoms, as shown in figure 2. Single-walled carbon nanotubes tend to adhere strongly to each other forming ropes or bundles of nanotubes as shown in figure 3 exhibiting physical properties of both metallic and semiconducting materials.

Carbon nanotubes exhibit promising mechanical and electrical properties. Tables 1 and 2 summarize mechanical and electrical properties of carbon nanotubes. It also compares properties with that of silicon, currently used material in CMOS technologies.

Metallic carbon nanotubes conduct an extremely large amounts of current densities. This property is what allows the application of metallic CNTs in interconnection substituting to metal wires, such as Cu, for the next generation of integrated circuits. On the other hand, semiconducting CNTs can be switched on and off by using a gate electrode. This property is what allows the application of CNTs in implementing field-effect transistors.

Single-walled carbon nanotubes have risen as one of the most likely candidates for miniaturizing electronics beyond current technology. The most fundamental application of metallic SWCNTs is in interconnection. Since it is difficult to prepare metallic CNT, fabrication and process integration of MWCNTs and CNT bundles interconnects have been reported in literature. The focus is on CNT-FETs and CNT interconnects made using semiconducting and metallic SWCNTs, respectively, and on some basic circuits, such as the inverter and ring oscillator which are composed of complementary CNT-FETs and CNT interconnects.

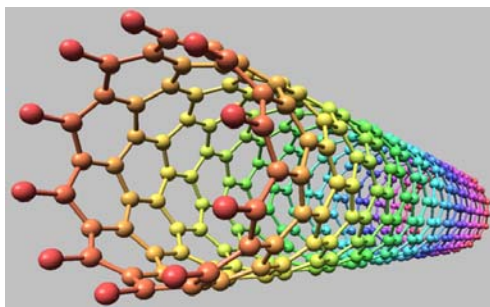


Figure 1 Single-walled carbon nanotube (Nanotube Modeler Software)

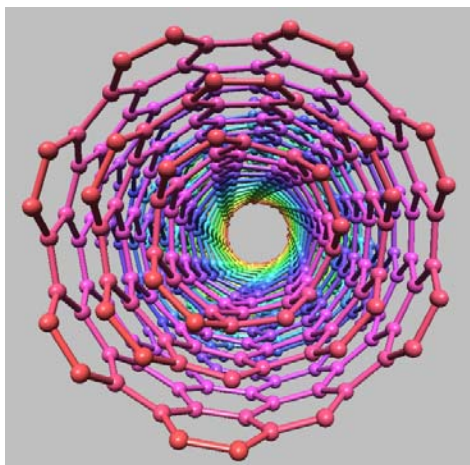


Figure 2 Multi-walled carbon nanotubes (Nanotube Modeler Software)

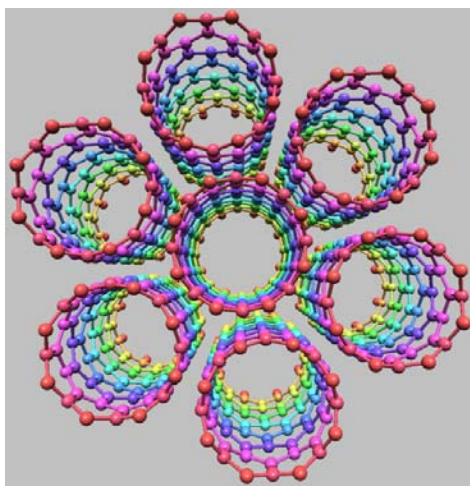


Figure 3 Single-walled carbon nanotubes bundle (Nanotube Modeler Software)

Table 1 Mechanical properties of carbon nanotubes and comparison with other materials

Material	Young's Modulus (TPa)	Tensile Strength (GPa)	Elongation at Break (%)	Thermal Conductivity (W/mK)
SWCNT	1-5	13-53	16	3,500-6,600
MWCNT	0.27-0.95	11-150	8.04-10.46	3000
Stainless Steel	0.186-0.214	0.38–1.55	15-50	16
Kevlar	0.06–0.18	3.6–3.8	~2	~1
Copper	0.11–0.128	0.22		385
Silicon	0.185	7		149

Table 2 Electrical properties of carbon nanotubes and comparison with other materials

Semiconductor					Metal		
Parameter	Semiconducting SWCNT	Silicon	GaAs	Ge	Parameter	Metallic SWCNT	Copper
Bandgap (eV)	0.9/diameter	1.12	1.424	0.66	Mean Free Path (nm)	1,000	40
Electron Mobility (cm ² /Vs)	20,000	1,500	8,500	3,900	Current density (A/cm ²)	10 ¹⁰	10 ⁶
Electron Phonon Mean Free Path (Å)	~700	76	58	105	Resistivity (Ω·m)	~10 ⁻⁵	1.68×10 ⁻⁸

2.3 Properties of Single-Walled Carbon Nanotubes

Single-walled carbon nanotubes can be characterized by its chirality or chiral vector. The chirality is an adapted concept uniquely of each type of nanotube that determines its properties and diameter. The chirality is represented with a pair of indices (n,m) called the chiral vector, which is shown in figure 4. The chiral vector traces the CNT around its circumference from one carbon atom (called the reference point) back to itself. It is expressed as,

$$\vec{C}_h = n\vec{a}_1 + m\vec{a}_2, \quad (1)$$

where \vec{a}_1 and \vec{a}_2 are the unit vectors for the graphene hexagonal structure and (n,m) are integers that represent the number of hexagons away from the reference point to the point, which will overlap to the reference point after rolled over, in the a_1 and a_2 directions, respectively. Using n, m indices CNTs can be classified in three groups: armchair nanotubes for $n = m$, zigzag nanotubes for $m = 0$ or $n = 0$, and chiral nanotubes for any other combination. Furthermore, integers n, m

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also determine whether a CNT is metallic or semiconducting, when $n - m = 3l$ (l is an integer), the nanotube is metallic, and when $n - m \neq 3l$, the nanotube is semiconducting. The energy gap of the semiconducting CNT depends on its diameter and is described as follows,

$$E_{gap} = 2V_{pp\pi}a_{c-c} / d, \quad (2)$$

where $V_{pp\pi}$ is Slater–Koster π tight-binding matrix element which is one of the Slater–Koster parameters for sp^3 tight-binding, a_{c-c} is the nearest neighbor distance between C-C bonds (0.142 nm) and d is the diameter of the CNT, which can be calculated using the following equation,

$$d = \sqrt{3} a_{c-c} \sqrt{n^2 + mn + m^2} / \pi \quad (3)$$

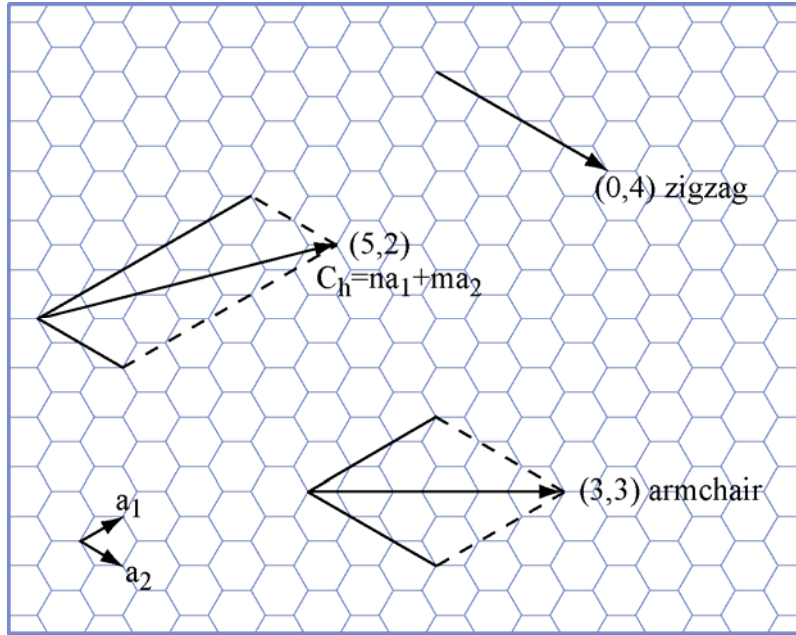


Figure 4 Schematic representation of a chiral vector in the crystal lattice of a carbon nanotube

2.3.1 Electronic Band Structure

Crystal Lattice and Reciprocal Lattice

Lattice is used to describe arrangement of atoms or molecules in a crystalline liquid or solid. The primitive cell of a carbon nanotube lattice can be described from the unit vectors:

$$\bar{a}_1 = \frac{a}{2}(\sqrt{3}\hat{x} + \hat{y}) \quad \text{and} \quad \bar{a}_2 = \frac{a}{2}(\sqrt{3}\hat{x} - \hat{y}), \quad (4)$$

where \bar{a}_1 and \bar{a}_2 are the unit cell vectors and a is the lattice constant, $a = \sqrt{3} \text{ a.c.}$

The reciprocal lattice is a lattice in the Fourier space associated with the crystal lattice. The reciprocal lattice vectors, \bar{b}_1 and \bar{b}_2 are given as follows:

$$\bar{b}_1 = \frac{2\pi}{a} \left(\frac{1}{\sqrt{3}} \hat{k}_x + \hat{k}_y \right) \quad \text{and} \quad \bar{b}_2 = \frac{2\pi}{a} \left(\frac{1}{\sqrt{3}} \hat{k}_x - \hat{k}_y \right) \quad (5)$$

Figure 5 shows plots of the crystal lattice structure and reciprocal lattice structure for a carbon nanotube with a chiral vector (4,3) generated using MATLAB from the chiral vector and the unit vectors from equations 4 and 5.

Energy Dispersion Relation

The energy dispersion relation defines relationship between the energy, E and wave vector, k . The energy dispersion relation for carbon nanotubes can be calculated from the electronic structure of graphene. The energy dispersion relation of a two-dimensional graphene is given by,

$$E_{2D}(\bar{k}) = \pm V_{pp\pi} \left\{ 3 + 2\cos(\bar{k} \cdot \bar{a}_1) + 2\cos(\bar{k} \cdot \bar{a}_2) + 2\cos[\bar{k} \cdot (\bar{a}_1 - \bar{a}_2)] \right\}^{1/2}, \quad (6)$$

where \bar{k} is the wave vector.

One-dimensional (1D) energy band can be derived from equation 6 for single-walled carbon nanotubes (SWCNTs) as follows,

$$E_{1D}(k) = \pm V_{pp\pi} \left\{ 1 + 4 \cos\left(\frac{\sqrt{3}k_x}{2}a\right) \cos\left(\frac{k_y}{2}a\right) + 4 \cos^2\left(\frac{k_y}{2}a\right) \right\}^{1/2}, \quad (7)$$

where the wave vectors k_x and k_y are obtained using the following relation,

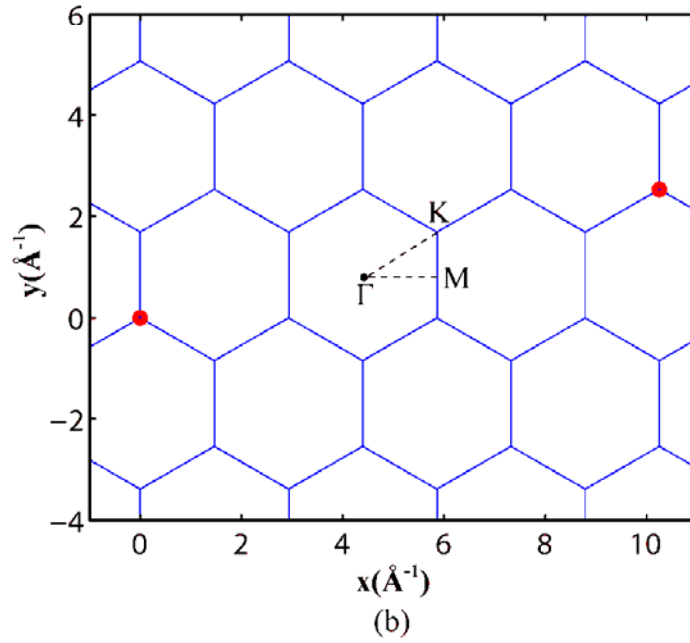
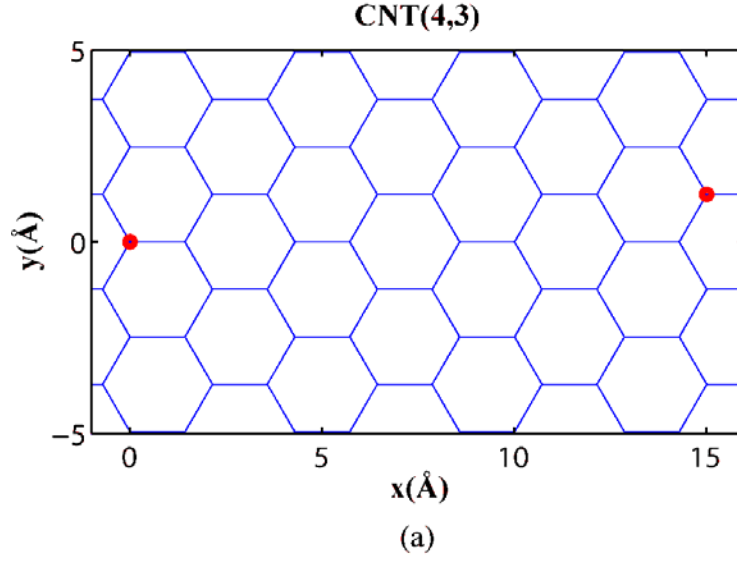


Figure 5 Schematic representation of (a) crystal lattice and (b) reciprocal lattice of a carbon nanotube with chiral vector (4,3)

$$\bar{k}(k_x, k_y) = \left(k \frac{\bar{K}_2}{|\bar{K}_2|} + q \bar{K}_1 \right) \quad \text{for } -\frac{\pi}{|T|} < k < \frac{\pi}{|T|} \text{ and } q = 1, \dots, N, \quad (8)$$

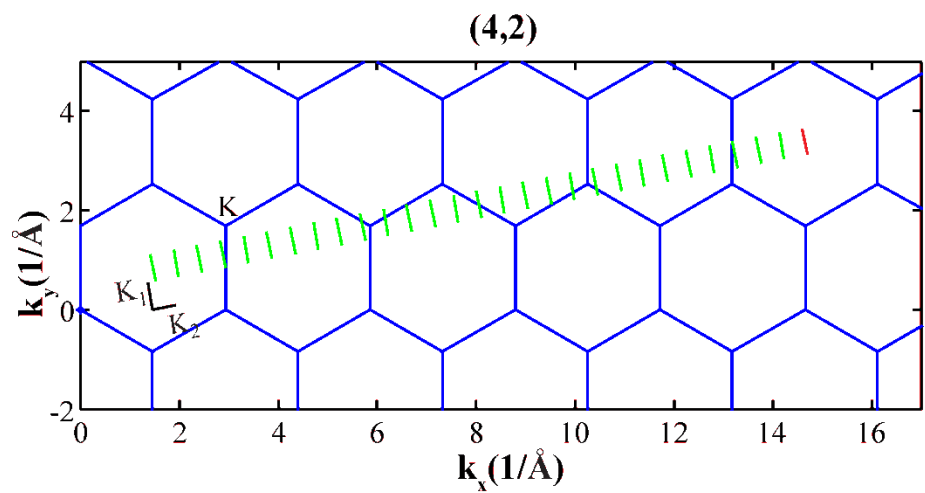
where k is the magnitude of the wave vector along the nanotube axis, $|T|$ is the magnitude of the translational vector and N is the number of hexagons within a unit cell. $|T|$ and N are given by,

$$|T| = \frac{\sqrt{3}\pi d_t}{d_R}, \quad N = \frac{2(n^2 + nm + m^2)}{d_R} \quad (9)$$

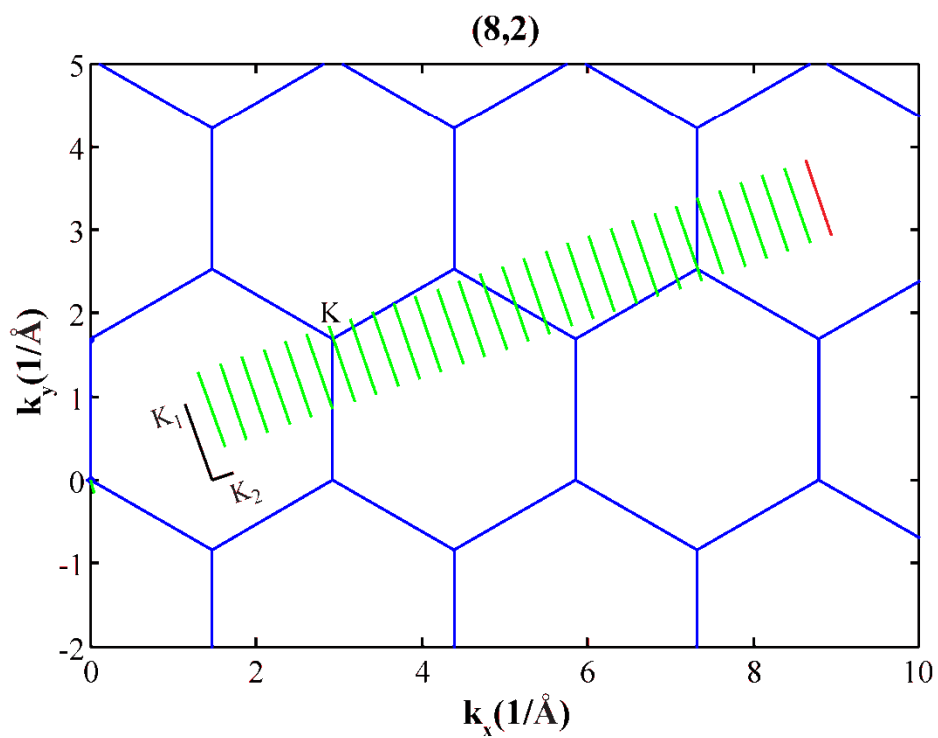
where d_R is the greatest common divisor of $(2n+m)$ and $(2m+n)$ and d_t is the diameter of the CNT. \bar{K}_1 and \bar{K}_2 denote the allowed reciprocal wave vectors along the tube and circumference axis given by,

$$\bar{K}_1 = \frac{(2n+m)\bar{b}_1 + (n+2m)\bar{b}_2}{Nd_R}, \quad \bar{K}_2 = \frac{m\bar{b}_1 - n\bar{b}_2}{N} \quad (10)$$

Figure 6 shows the plot of wave vector in k -space (momentum space) for a CNT with chiral vectors (a) (4,2) and (b) (8,2). The reciprocal Bravais lattices are lines, which mean that carbon nanotube is a one-dimensional (1D) material. Unlike CNT (4,2), the wave vector of CNT (8,2) passes through K point in the two-dimensional (2D) Brillouin zone of graphene. Figure 7 shows the plot of the energy band diagram in k -space for a CNT with chiral vectors (a) (4,2) and (b) (8,2).



(a)



(b)

Figure 6 Plot of the allowed wave vectors in k -space for a CNT with (a) chiral vector $(4,2)$ and (b) chiral vector $(8,2)$

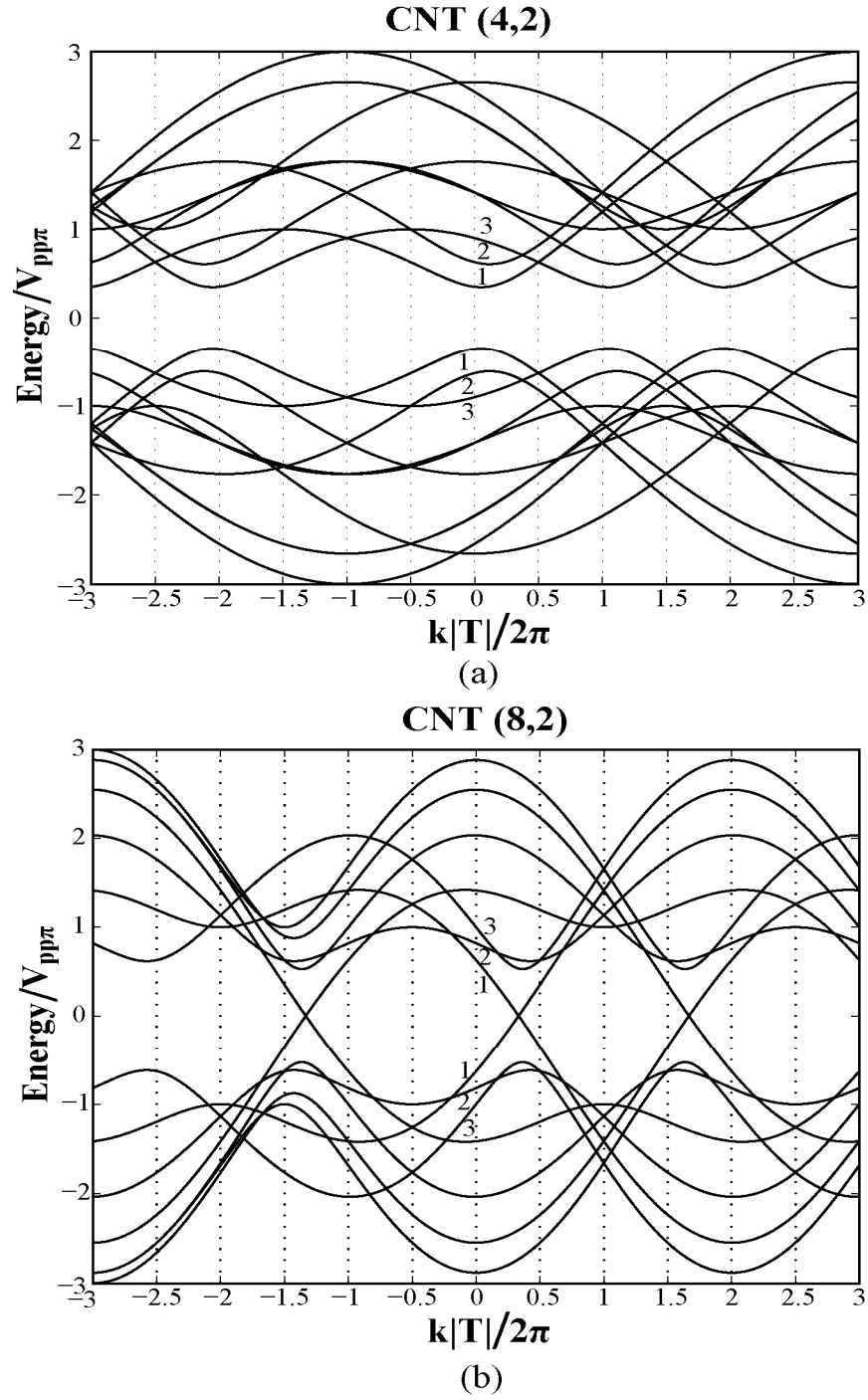


Figure 7 Plot of the energy band diagram in k -space for a CNT with (a) chiral vector (4,2) and (b) chiral vector (8,2)

2.3.2 Density of States

The k -vectors in momentum (k) space depend on vectors K_1 and K_2 are shown in figure 6. It also represents the area in the momentum space for each state (each single line), which is $A_p^{1\text{-state}} = \hbar^2 |K_1| |K_2| / 2$ and a differential area as $dA_p = \hbar^2 |K_1| dk$, where dk is in the direction of K_2 and \hbar is the Planck Constant (h) divided by 2π . The density of states per unit energy is obtained as follows,

$$D(E)dE = 2 \frac{dA_p}{A_p^{1\text{-state}}} = \frac{4}{\hbar^2 |K_1| |K_2|} \hbar^2 |K_1| \left| \frac{dk}{dE} \right| dE = \frac{2|T|}{\pi} \left(\frac{dE}{dk} \right)^{-1} dE \quad (11)$$

A combination of equation 7 for 1D energy dispersion and equation 11 for density of states can be used to plot the density of states for any chiral vector of carbon nanotube. Figure 8 shows density of states plots for a CNT (4,2) and CNT (8,2) obtained from MATLAB. Each peak in figure 8 is called a Van Hove Singularity and its respective energy represents a conduction energy-band minimum value. The total number of Van Hove Singularities is the number of bands a CNT has. There is a band gap in figure 8(a) which means the CNT (4,2) is semiconducting and there is a finite value of the density of states at the Fermi level in figure 8(b) which means the CNT (8,2) is metallic.

It is shown from figures 6,7 and 8 that the wave vectors of CNT (4,2) do not pass through K point in the 2D Brillouin zone of graphene, there is a band gap and there is no state in the band gap. Therefore, CNT (4,2) is a semiconductor. Some of the wave vectors of CNT (8,2) pass through K point in the 2D Brillouin zone of graphene, there is no band gap and there is a finite state in the band gap. Therefore, CNT (8,2) is metallic.

2.4 Applications of CNTs in Integrated Circuits

Whereas semiconducting CNTs found applications in making CNT-FETs, metallic CNTs have distinct advantages compared with metal wires for interconnection in integrated circuits.

2.4.1 Applications of Semiconducting Carbon Nanotubes

Studies have demonstrated that semiconducting CNTs have excellent electrical properties, including long mean free path ($\sim 0.7\mu\text{m}$) and high electron mobility. Experiments with CNT-FETs have further demonstrated that transistors based on semiconducting CNTs have large transconductance, which indicates a great potential for sub-nm integrated circuits.

It has been suggested that high- κ dielectrics are essential for future transistors due to low leakage currents and reduced power dissipation. However, a fundamental problem for conventional semiconductors is the degradation of electrical properties due to carrier scattering mechanisms introduced at the high- κ film semiconductor interface. Recently, it has been shown that CNT-FETs can be operated in ballistic range with high- κ dielectrics, thereby opening the door to ultrafast devices since both the ballistic transport of electrons and high- κ dielectrics facilitate high on-current that is directly proportional to the speed of a transistor.

Early CNT-FETs were fabricated on oxidized silicon substrates. The poor gate coupling due to the thick Silicon Dioxide (SiO_2) layer and back gate geometry limited their applications. However, in 2002, the implementation of top-gate geometry made the CNT-FET a more promising candidate for next generation field-effect transistors. Both n-type CNT-FETs and p-type CNT-FETs were made and demonstrated for performance similar to current MOSFETs. Additional improvements in the metal-CNT contact resistance at the source and drain ends have led improved CNT-FET performances. Now with improved processing techniques, CNT-FETs with very high ON/OFF switching ratio and high carrier mobility have been fabricated. In addition, fabrication of inverters which are composed of n-type and p-type CNT-FETs were also reported in. Recently, a doping-free fabrication method has been proposed for the CNT-based ballistic complementary metal-oxide semiconductor devices and circuits, which are compatible with current CMOS fabrication processes. This work may lead to the fabrication of complex CNT-based integrated circuits.

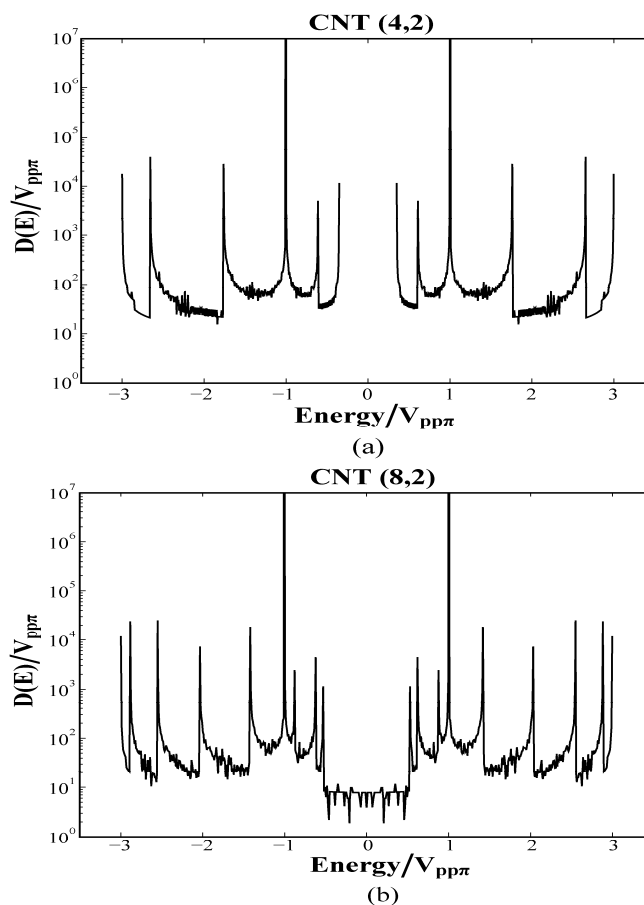


Figure 8 Plot of the density of states for a CNT with (a) chiral vector (4,2) and (b) chiral vector (8,2)

2.4.2 Applications of Metallic Carbon Nanotubes

Metallic CNTs have attracted significant attention because their current carrying ability is remarkable. Ballistic transport of electrons has been observed and values for the conductance that approaches the theoretical limit $(4e^2/h)^1$ have been measured at small biases. Metallic CNTs hold promise as interconnects in sub-nm CMOS circuits because of their low resistance and strong mechanical properties. An emerging problem with interconnects in sub-nm CMOS technology is the breakdown of copper wires due to electromigration when current densities exceed 10^6 A/cm². Preliminary work have shown that an array of nanotubes can be integrated with silicon technology and holds promise as vertical vias to carry more than an order of magnitude larger current densities than conventional vias. It has been demonstrated that MWCNTs can carry current densities approaching 10^{10} A/cm². Metallic CNTs are excellent wires, with near-perfect experimentally measured conductance. This is because surface scattering, disorder, defects and phonon scattering, which lead to a decrease in conductance, have negligible effects in metallic CNTs, especially when the size of the conductor is shrinking. The reasons for this are the following.

The acoustic phonon mean free paths in CNTs are longer than a micron. The dominant scattering mechanisms are due to zone boundary and optical phonons with energies of approximately 160 and 200 meV; but scattering with these phonons at room temperature is ineffective at small biases.

In a silicon field effect transistor, there is significant scattering of electrons due to the disordered nature of the Si-SiO₂ interface. However, the CNT has a crystalline surface without disordered boundaries.

Any potential that is long-ranged compared with the CNT lattice constant will not effectively couple the two crossing sub-bands because of lack of wave vector components in the reciprocal space.

The electrons in the crossing sub-bands of carbon nanotubes have a large velocity of 8×10^5 m/s at the Fermi energy. There are only two sub-bands at the Fermi energy. These two facts make the electron reflection probability due to disorder and defects small.

2.5 Synthesis of Carbon Nanotubes

At present carbon nanotubes are being synthesized using the following techniques: arc discharge, laser ablation, high-pressure carbon monoxide (HiPCO) and CVD methods.

Arc discharge, laser ablation and CVD are popular methods to produce CNTs. Arc discharge method creates CNTs through arc vaporization of two carbon rods placed end to end, separated by a small gap (~mm), in an enclosure that is usually filled with inert gas at low pressure. In this method, carbon nanotubes are produced at the cathode crater. Laser ablation can be carried out in a horizontal flow tube under a flow of inert gas at controlled pressure. In this set-up, the flow tube is heated to ~1200°C by a tube furnace. Laser pulses enter the tube and strike a target consisting

¹ $4e^2/h = 155\mu S$

of a mixture of graphite and a metal catalyst such as Co, Pt, Ni, Cu, etc. Carbon nanotubes condense from the laser vaporization plume and are deposited on a collector sitting outside of the furnace. Arc discharge and laser ablation are modified physical vapor deposition (PVD) techniques and are high temperature and low production processes, which are more suitable for laboratory research. Chemical vapor deposition (CVD) has become the most important commercial approach for synthesis of CNTs. It is also suitable to produce on-chip nanotubes directly, which provides a convenient way for further device fabrication. First, the gaseous carbon molecules, such as methane or carbon monoxide are heated in a furnace and break into atomic carbons. Then the atomic carbons diffuse toward the substrate coated with catalyst particles forming carbon nanotubes. Carbon nanotube synthesis by CVD is essentially a two-step process. The first step is a preparation of patterned catalyst, such as clusters of Ni, Fe and Co. The next step is a synthesis of the nanotube by heating up the substrate in a carbon rich gaseous environment. In all of these methods, the generation of free carbon atoms and the precipitation of dissolved carbon from catalyst particles are involved. The growth terminates when the catalyst particle gets poisoned by the impurities or the stable metal carbide is formed.

Besides these three popular methods, there are other proposed methods to synthesize CNTs, such as flame synthesis and HiPCO. Recent work has shown that flame synthesis is an inexpensive large-scale method to produce single-walled carbon nanotubes. In a flame synthesis process, the hydrocarbon fuel combusts to generate enough heat to trigger the process, and to form small aerosol metal catalyst islands. Single-walled carbon nanotubes grow in these catalyst islands in the same way as in the arc discharge and laser ablation processes.

SWCNTs of high quality can also be produced for very high selectivity and with a remarkably narrow distribution of tube diameters. The technique is based on a unique Co-Mo catalyst formulation that inhibits the formation of undesired forms of carbon. During the reaction, cobalt is progressively reduced from the oxidic state to the metallic form. The strategy used in this method is to keep the active cobalt stabilized in a non-metallic state by interaction with molybdenum oxide (MoO_3). When exposed to carbon monoxide, the Co-Mo dual oxide is carburized, producing molybdenum carbide (Mo_2C) and small metallic Co clusters, which remain in a high state of dispersion and result in high selectivity towards SWCNT of very small diameter.

This catalytic synthesis of SWCNTs uses a continuous-flow gas phase using CO as the carbon source and $\text{Fe}(\text{CO})_5$ as the iron-containing catalyst precursor. Single-walled carbon nanotubes are synthesized when the two gases flow through a heated reactor. Diameter of the nanotubes can be roughly selected by controlling the pressure of carbon monoxide (CO). Single-walled carbon nanotubes with 0.7 nm in diameter, which are expected to be the smallest SWCNTs, have been produced by this method.

2.6 CNT Based Circuit Modeling

As discussed in Section 2.4, CNT-FETs and metallic CNT wires show performance metrics significantly above those of Si MOSFETs and metal interconnect wires, respectively. SWCNT CNT-FETs have been fabricated in which MWCNTs are used as local interconnects, making a successful first step towards CMOS circuits fabricated entirely from carbon nanotubes. However, studies of individual CNT-FET and CNT wire are not comprehensive enough to enable

conclusions about development of large-scale CNT based integrated circuits. The viability of CNT-FET circuits depends on the behavior of logic gates that are composed of multiple CNT-FETs and used in larger scale circuits. Therefore, circuit models including device models and interconnects model are necessary to predict the behavior of CNT based circuits. Furthermore, like the great help by the CMOS models in optimization of CMOS circuits design, it will be helpful to optimize the CNT based circuits design by utilizing the CNT-FET and CNT interconnect models. As a result, CNT-FET modeling and CNT interconnects modeling are the current focus of most active research in CNT based integrated circuits design.

2.6.1 CNT-FET Modeling

A good amount of work on modeling CNT-FETs has been reported. However, these models are still numerical-based and require a mathematical/software realization. Recently, we have obtained an analytical solution of current transport model for the CNT-FET for analysis and design of CNT-FET based integrated circuits. In our work, we have used Verilog-AMS (Analog Mixed-Signal) to describe the CNT-FET static and dynamic models and simulated CNT-FET circuits using Cadence/Spectre. Verilog-AMS requires less computational steps and easy to experiment with the developing model equations.

2.6.2 CNT Interconnect Modeling

A model describing the electromagnetic field propagation along a CNT is indispensable in order to study the interconnection performance of CNT while comparing with traditional metal interconnects. Three theories are used to build different models. Luttinger Liquid Theory describes interacting electrons (or other fermions) in one-dimensional conductor and is necessary since the commonly used Fermi liquid model breaks down in one-dimension. Burke regards that electrons are strongly correlated when they transport along the CNT and proposed a transmission line model based on the Luttinger Liquid Theory. Another transmission line model was built based on Boltzmann Transport Equation (BTE). Two-dimensional electron gas, where the charged particles are confined to a plane and neutralized by an inert uniform rigid positive plane background was studied by Fetter. Based on the work of Fetter, Maffucci et al. investigated electron transport along the CNT and proposed a third model, fluid model. The first model is based on quantum dynamics concepts; the second model requires solving the Boltzmann Transport Equation; the third model has been developed within the framework of the classical electrodynamics and is simple on concepts and mathematical modeling.

3. METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Introduction

Current transport and dynamic models of carbon nanotube field-effect transistors are presented. A model of single-walled carbon nanotube as interconnects is also presented and extended in modeling of single-walled carbon nanotube bundles. These models are applied in studying the performances of circuits such as the complementary carbon nanotube inverter pair and carbon nanotube as interconnect. Cadence/Spectre simulations show that carbon nanotube field-effect transistor circuits can operate at upper GHz frequencies. Carbon nanotube interconnects give smaller delay than copper interconnects used in nanometer CMOS VLSI circuits.

In a recent work, we have made modification in two-dimensional fluid model to include electron-electron repulsive interaction and built a semi-classical one-dimensional fluid model, which is relatively easy to solve and apply in CNT transmission line modeling. We have also proposed circuit models for SWCNT bundles as interconnects based on the one-dimensional fluid model.

3.1.1 CNT-FET Static model

The structure of a CNT-FET shown in figure 9 is similar to the structure of a typical MOSFET, where a SWCNT forms the channel between two electrodes, which work as the source and drain of the transistor. The structure is built on top of an insulating layer and a substrate which works as the back gate. The top gate is metal over the thin gate oxide. Current transport equations in a CNT-FET are developed which are described here as follows and include both drift current and diffusion currents.

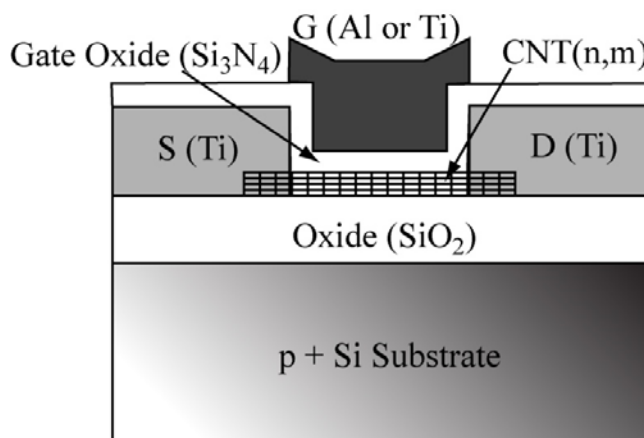


Figure 9 Vertical cross-section of a CNT-FET.

$$\begin{aligned}
I_{ds} &= I_{drift} + I_{diff} \\
&= \beta \left[f_{drift} \left\{ \Psi_{cnts}(L), V_{gs} \right\} - f_{drift} \left\{ \Psi_{cnts}(0), V_{gs} \right\} \right] + \\
&\quad + \beta \left[f_{diff} \left\{ \Psi_{cnts}(L), V_{gs} \right\} - f_{diff} \left\{ \Psi_{cnts}(0), V_{gs} \right\} \right],
\end{aligned} \tag{12}$$

where

$$\begin{aligned}
f_{drift}(\psi_{cnts}(x), V_{gs}) &= (V_{gs} + V_{sb} - V_{fb}) \psi_{cnts}(x) - \frac{1}{2} \psi_{cnts}^2(x) \\
f_{diff}(\psi_{cnts}(x), V_{gs}) &= \frac{kT}{q} \psi_{cnts}(x) \\
\beta &= \gamma \frac{\mu C_{oxl}}{L^2}
\end{aligned} \tag{13}$$

In equations 12 and 13, various parameters are defined as follows: L : gate length, μ : carrier mobility, k : Boltzmann constant, T : temperature, °K, V_{fb} : flat-band voltage, V_{gs} : gate-source voltage, V_{sb} : source-substrate voltage, ψ_{cnts} : surface potential of CNT, C_{oxl} : gate-oxide capacitance per unit area. For a carbon nanotube of length L and radius r in a CNT-FET, the oxide capacitance is given by,

$$C_{oxl} = 2\pi\epsilon_{oxl}L / \ln \left(\frac{T_{oxl} + r + \sqrt{T_{oxl}^2 + 2T_{oxl}r}}{r} \right). \tag{14}$$

In equation 14, T_{oxl} is the thickness of the gate oxide and r is the radius of the CNT. Equation 12 is modified to incorporate channel length modulation through the parameter, λ as in a MOSFET. In saturation region, modified equation 12 is described as follows,

$$I_{ds} = \beta \left[f(\psi_{cnts}(L), V_{gs}) - f(\psi_{cnts}(0), V_{gs}) \right] (1 + \lambda V_{ds}). \tag{15}$$

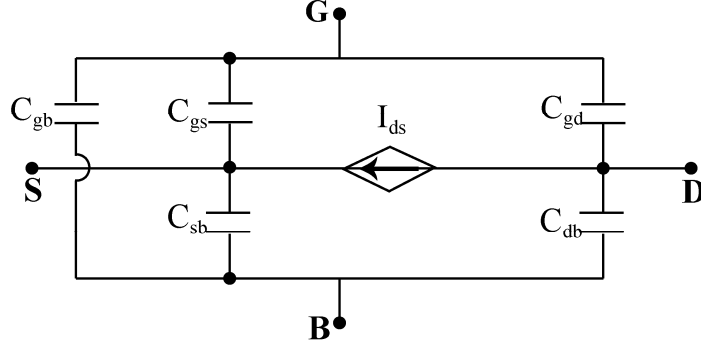


Figure 10 Meyer capacitance model for CNT-FETs

3.1.2 CNT-FET Dynamic Model

The dynamic response of a CNT-FET can be modeled using Meyer capacitance model as shown in figure 10. Recently, we have obtained capacitances, C_{gs} , C_{gd} and C_{gb} based on current transport modeling of CNT-FETs described by equation 12, which are as follows:

In linear region:

$$C_{gb} = 0, \quad (16a)$$

$$C_{gs} = -\frac{\gamma\mu W|C_h|C_{ox1}^2}{2\beta} \cdot \frac{\left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs}) \right] \left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{2}{3}V_{gd} - \frac{1}{3}V_{gs}) \right]}{\left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs}) \right]^2}, \quad (16b)$$

$$C_{gd} = -\frac{\gamma\mu W|C_h|C_{ox1}^2}{2\beta} \cdot \frac{\left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs}) \right] \left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{3}V_{gd} - \frac{2}{3}V_{gs}) \right]}{\left[\delta I e^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs}) \right]^2}, \quad (16c)$$

In saturation region:

$$C_{gb} = 0, \quad (17a)$$

$$C_{gs} = \frac{1}{3} \frac{\gamma\mu W|C_h|C_{ox1}^2}{\beta}, \quad (17b)$$

$$C_{gd} = 0, \quad (17c)$$

Considering C_{sb} and C_{db} to be equal to one half the insulator capacitance, $C_{ox2}/2$ in series with the depletion-layer capacitance, $C_{subs}/2$, we obtain,

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$$C_{ox2} = 2\pi\epsilon_{ox2}L \left/ \ln \left(\frac{T_{ox1} + r + \sqrt{T_{ox2}^2 + 2T_{ox2}r}}{r} \right) \right., \quad (18)$$

$$C_{subs} = \frac{N_A q \epsilon_s + \sqrt{N_A q \epsilon_s} \sqrt{8C_{ox2}^2 V_{gb} + N_A q \epsilon_s - 8C_{ox2}^2 \phi_{ms} - 8C_{ox2}^2 \psi_{cnt}}}{4C_{ox2} (V_{gb} - \phi_{ms} - \psi_{cnt})}, \quad (19)$$

where ϵ_s is the permittivity of the semiconductor, W_s is the depletion region width and N_A is the doping concentration.

3.1.3 SWCNT Interconnect Model

Figure 11 shows the geometry of a SWCNT interconnect. Based on two-dimensional fluid model. We have proposed one-dimensional fluid model to describe the electron transport in metallic CNT and built a transmission line model of metallic CNT interconnects. When compared with a two-dimensional fluid model, one-dimensional fluid model is accurate and takes into account electron-electron interaction. The Luttinger Liquid Theory models SWCNT as a one-dimensional conductor from quantum concept and take into account electron-electron correlation. However, our model is simple in mathematical modeling and easier to extend in modeling of CNT bundles as interconnections. The basic equation is Euler's equation, which is the Newton's Second Law applied in fluid dynamics and is given by,

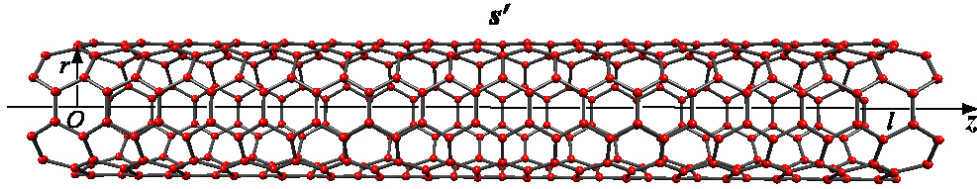


Figure 11 Geometry of a single wall carbon nanotube (SWCNT)

$$mn \left(\frac{\partial}{\partial t} + v_z \frac{\partial}{\partial z} \right) v_z = - \frac{\partial p}{\partial z} - en \{ (1 - \alpha) \mathcal{E}_z |_{s'} \} - mn \nu v_z, \quad (20)$$

where n_0 is the equilibrium electron density, v_z is the electron mean velocity, p is the pressure, m is the electron mass, e is the electronic charge and \mathcal{E}_z is electric field. The second term on the right hand side represents Lorentz force and includes electron-electron interaction through the parameter, α . The last term on the right hand side represents the effect of scattering of electrons with the positive charge background and ν is the electron relaxation frequency, $\nu = v_F / l_{mfp}$, where l_{mfp} is the mean-free path of electron in CNT and v_F is the Fermi velocity. Length of CNT is l and

$sgn(l)$ is the sign function defined as follows, $sgn(l) = \begin{cases} 0 & \text{if } l < l_{mfp} \\ 1 & \text{if } l \geq l_{mfp} \end{cases}$. The parameter, α

describes the classical electron-electron repulsive interaction given by:

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$$\alpha \equiv \frac{\mathcal{E}_{zP}}{\mathcal{E}_z} = \frac{E_P}{E} = \frac{E_P}{E_K + E_P}, \quad (21)$$

where \mathcal{E}_{zP} is the part of the electrical field which provides potential energy to electrons in z -direction. E is the total energy of electrons. E_P and E_K are the potential and kinetic energies of electrons, respectively.

The equation relating current density, charge density and electric field can be described as follows ,

$$\frac{\partial j(z,t)}{\partial t} + vj + u_e^2 \frac{\partial \sigma(z,t)}{\partial z} = \frac{e^2 n_0}{m} (1 + \alpha) \mathcal{E}_z. \quad (22)$$

We consider a metallic single-walled CNT above a perfect conducting plane and assume that the propagating EM wave is in quasi-TEM mode. The voltage and current intensity are then expressed as follows,

$$i(z,t) = \oint \vec{j} \cdot \vec{z} dl \approx 2\pi r j(z,t), \quad (23)$$

$$q(z,t) = \oint \vec{\sigma} \cdot d\vec{l} \approx 2\pi r \sigma(z,t). \quad (24)$$

Combining equations 23 and 24, following equation is obtained,

$$\mathcal{E}_z = Ri + L_K \frac{\partial i}{\partial t} + \frac{1}{C_Q} \frac{\partial q}{\partial z}, \quad (25)$$

where $R \equiv L_K \text{sgn}(l)v$ is the resistance per unit length of CNT, $L_K \equiv m/[(1+\alpha)2\pi e^2 n_0]$ is the kinetic inductance per unit length and $C_Q \equiv 1/L_K u_e^2$ is quantum capacitance per unit length and $u_e = \frac{v_F}{\sqrt{1-\alpha}}$, is the thermodynamic speed of sound of the electron fluid under neutral environment.

The magnetic inductance and electric capacitance per unit length of a perfect conductor on a ground plane are given by,

$$L_M = \frac{\mu}{2\pi} \cosh^{-1}\left(\frac{h}{r}\right) \approx \frac{\mu}{2\pi} \ln\left(\frac{h}{2r}\right), \quad (26)$$

$$C_E = \frac{2\pi\epsilon}{\cosh^{-1}(h/r)} \approx \frac{2\pi\epsilon}{\ln(h/r)}, \quad (27)$$

where h is the distance of CNT to the ground plane. Equations 26 and 27 are accurate enough for $h > 2r$.

3.1.4 SWCNT Bundle Interconnect Model

Carbon nanotube can also be fabricated in bundles. The spacing between nanotubes in the bundle is due to the van der Waals forces between the atoms in adjacent nanotubes. One of the most critical challenges in realizing high-performance SWCNT interconnect is in controlling the proportion of metallic nanotubes in a bundle. Current SWCNT fabrication techniques cannot effectively control the chirality of the nanotubes in a bundle. Therefore, SWCNT bundles have metallic nanotubes that are randomly distributed within the bundle. It has been shown that metallic nanotubes are distributed with a probability, $\beta = 1/3$ in a growth process.

Figure 12 shows the cross-section of a SWCNT bundle. Since the van der Waals force between the carbon atoms in adjacent SWCNTs is negligible compared to covalent bond between carbon atoms in a SWCNT, the one-dimensional fluid model can be applied to the each SWCNT in the bundle with modification.

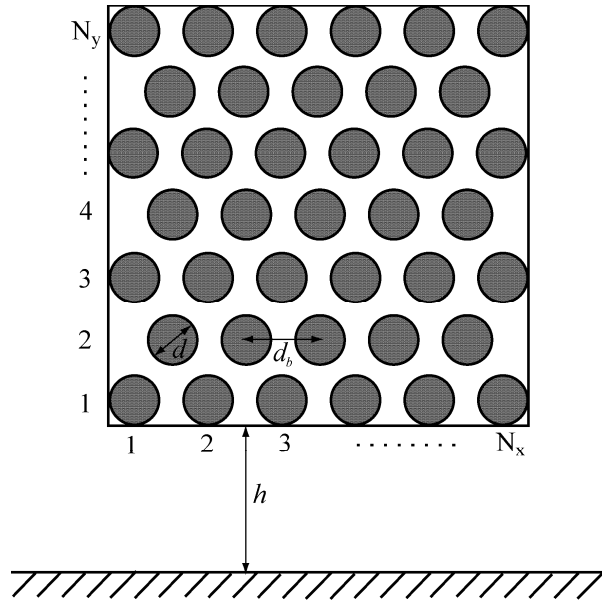


Figure 12 Cross-section of SWCNT bundle interconnect wire

Considering one of the SWCNTs, assuming electrons in SWCNT will be only affected by the electrons in the adjacent metallic SWCNTs and semiconducting SWCNTs have no effect on the conductance of the bundle. To calculate the potential energy, we first consider the potential energy of each SWCNT and then move them adjacent to each other to compose the SWCNT bundle. Average potential energy of electrons in a single SWCNT can be described by the following equation:

$$E_P = 6 \frac{e^2}{2\pi\epsilon_0} \frac{1}{d} + \beta \sum_{i=1}^{\Gamma} \frac{16e^2}{2\pi\epsilon_0} \frac{1}{d_b} \quad (28)$$

where d is diameter of CNT and $d_b = \delta + d$ is the distance of the adjacent SWCNT shown in figure 12. δ is the spacing between the SWCNT in the bundle corresponds to the van der Waals distance between graphene layers in graphite. Γ is the average number of SWCNTs neighboring a SWCNT. The number of SWCNTs neighboring to the corner SWCNT is 2, the number of SWCNTs neighboring to the edge SWCNT is 4 and the number of SWCNTs neighboring to the inside

SWCNT is 6. Therefore, $\Gamma = \left\lfloor \frac{6N_x N_y - 4N_x - 4N_y - 2[N_y/2]}{N_x N_y - 2[N_y/2]} \right\rfloor$, where the square brackets is a

floor function.

The kinetic energy of the electrons is described by:

$$E_K = 4 \times \frac{1}{2} m v_F^2 \approx 7 \text{ eV} \quad (29)$$

Therefore, electron-electron interaction parameter α for SWCNT bundle can be calculated. Total number of metallic SWCNTs in a bundle can be described by $N = \beta(N_x N_y - [N_y/2])$. Following the derivation of electric field and current charge relation, we get the similar equation for the electric field as described below:

$$\mathcal{E}_z = Ri + L_K \frac{\partial i}{\partial t} + \frac{1}{C_Q} \frac{\partial q}{\partial z} \quad (30)$$

where $R \equiv L_K \text{sgn}(l)\nu$ is one SWCNT resistance in a SWCNT bundle per unit length.

$L_K \equiv \frac{\pi\hbar}{4e^2 v_F}$ is one SWCNT kinetic inductance per unit length and $C_Q \equiv \frac{1}{L_K u_e^2}$ is one SWCNT

quantum capacitance per unit length. And $u_e = \frac{v_F}{\sqrt{1-\alpha}}$, is the thermodynamic speed of sound of the electron fluid under a neutral environment.

The SWCNTs at the bottom shield the upper SWCNTs from the ground plane. Therefore, the electric capacitance does not exist in the upper SWCNTs. However, there exists electric capacitance per unit length, C_b , between the neighboring metallic SWCNTs and its value is given by:

$$C_b = \frac{\pi\epsilon_0}{\ln \left(\frac{d_b}{d} + \sqrt{\left(\frac{d_b}{d} \right)^2 - 1} \right)} \quad (31)$$

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Figure 13 shows the equivalent circuit of a SWCNT bundle as an interconnect wire. $N_b = N_x$, is the number of lowest level metallic SWCNTs, which shield upper levels SWCNTs from ground plane. $N_a = N - N_b$, is the number of upper levels metallic SWCNTs.

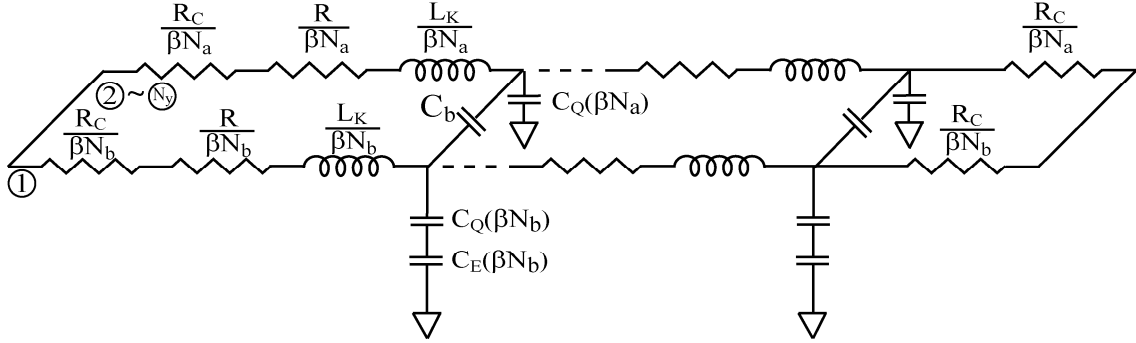


Figure 13: Equivalent circuit of SWCNT bundle interconnect.

3.1.5 Results and Discussion

We have developed analytical CNT-FET models for I-V characteristics and verified with the experimentally measured I-V characteristics. Table 3 summarizes some of the physical and electrical parameters of CNT-FETs and comparison with equivalent MOSFET parameters. It is noticed from table 3 that the CNT-FET carries a higher current density compared with the equivalent bulk silicon and silicon on insulator (SOI) MOSFETs. In the following, we have used our CNT-FET models in studying the performance of a ring oscillator circuit and compared with the measured performance.

Table 3 A comparison of modeled and measured parameters of CNT-FET and MOSFETs

FET Parameters	p-type CNT-FET* Model	p-type CNT-FET* Measured	Bulk-Si p- MOSFET Measured	SOI p- MOSFET Measured
Gate Length (nm)	260	260	15	50
Gate Oxide Thickness (nm)	15	15	1.4	1.5
Threshold Voltage (V)	- 0.3	- 0.5	~ - 0.1	~ - 0.2
Subthreshold Swing (mV/dec)	110	130	100	70
On-Current per unit Width ($\mu\text{A}/\mu\text{m}$)	2000	2100	265	650

*Chiral Vector: (11, 9)

Figure 14(a) shows schematic of a five stage ring oscillator circuit. Figure 14(b) shows the simulation result of the ring oscillator output waveform at 0.92 V supply voltage. Figure 14(c) shows the oscillation frequency with varying supply voltage. The modeled curve does not include the effect of channel length modulation. Dimensions of both the n- and p-type CNT-FETs are: $d = 2$ nm and $L = 600$ nm. Modeled and experimental curves show that the frequency of the ring oscillator is about 70-80 MHz at 1.04 V supply voltage. The frequency is low because CNT-FETs in this ring oscillator are 600 nm long and there are parasitic capacitances associated with the metal wire in the ring oscillator. Shorter length of CNT-FETs will increase the oscillating frequency as shown in figure 15.

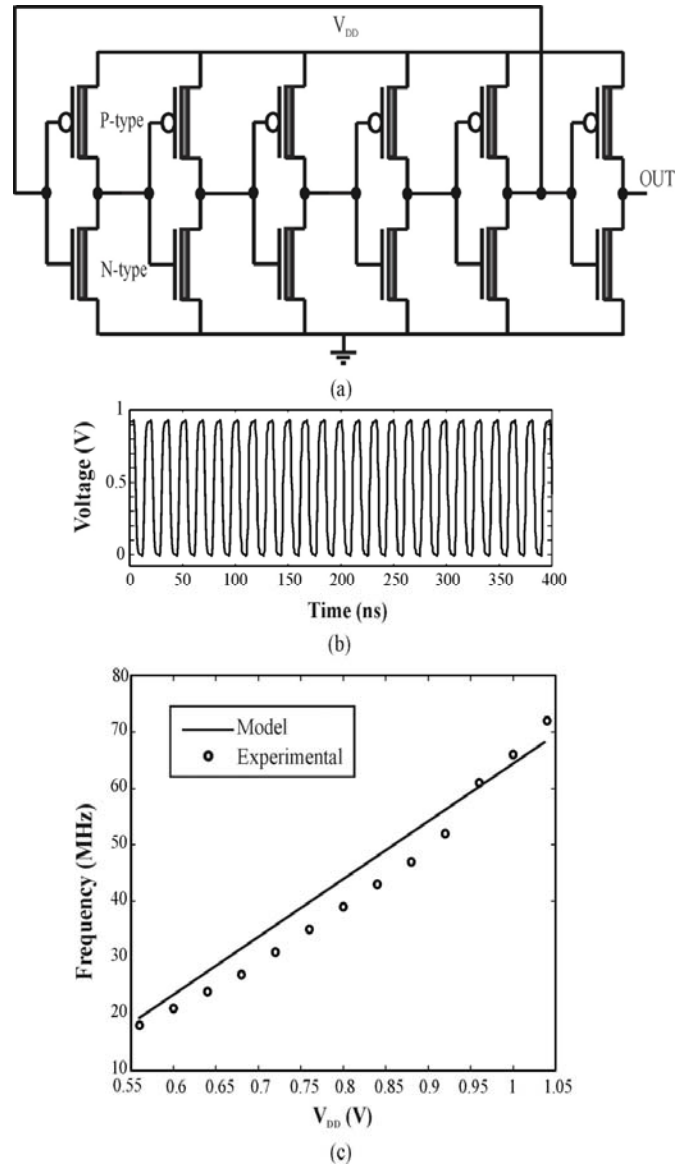


Figure 14 (a) Schematic of a 5-stage ring oscillator, (b) output waveform of ring oscillator and (c) oscillating frequency versus supply voltage, V_{DD}

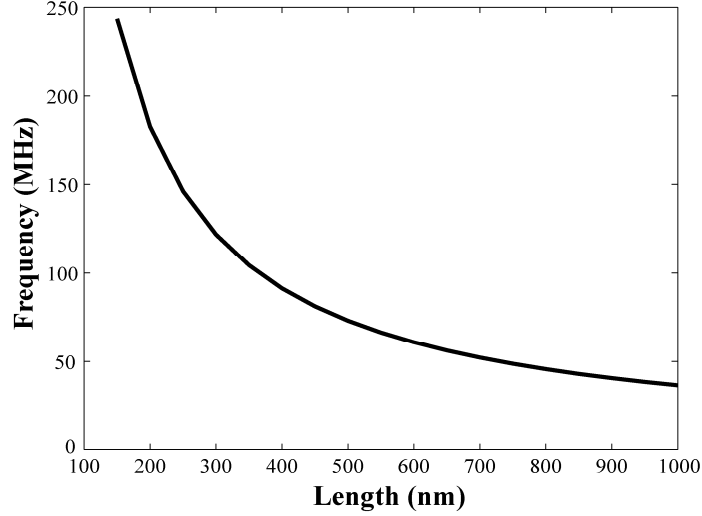


Figure 15 Oscillating frequency of a 5-stage ring oscillator versus length of the CNT-FETs

SWCNT exhibits large contact resistance when used as an interconnect wire. However, CNT bundle gives low contact resistance when used as the circuit interconnect wire. Contact resistance in a bundle, however, will depend on the number of SWCNTs being metallic. Utilizing the models of CNT interconnects we have also studied the performance of CNT-FET circuit inverter pair with different kinds of interconnects including the copper. One of the advantages of CNT interconnect is its large mean free path, l_{mfp} , which is on the order of several micrometers (as compared to 40 nm for Cu at room temperature). It provides low resistivity and ballistic transport in short-length interconnects. In this work, first we have simulated a CNT-FET inverter pair with $0.1 \mu\text{m}$ Cu and SWCNT bundle as interconnect wires using Cadence/Spectre. We have utilized the process parameters from the 2016 node, 22nm technology and assumed a 22 nm width and 44 nm height of the SWCNT bundle. The spacing between nanotubes in the bundle is due to van der Waals forces between the atoms in adjacent nanotubes, which mean the spacing between adjacent SWCNTs is 0.34 nm. If we assume diameter of a SWCNT in a bundle is to be 1 nm then there are nearly 500 SWCNTs in the 22 nm (width) \times 44 nm (height) bundle following figure 12.

Figure 16 shows input and output waveforms of a CNT-FET inverter pair using SWCNT bundle as an interconnect wire and comparison with the ideal interconnect ($RC=0$) and Cu interconnect. Input signal is a 4 GHz square wave pulse. The average delay is 6 ps, which suggests that the CNT-FET inverter pair can respond up to 100 GHz input signal. The performance of SWCNT bundle as an interconnect wire ($\beta=1$) is close to Cu interconnect. It is due to contact resistance and relatively larger capacitance in a SWCNT bundle. The average delays are smaller for $\beta=1$ than that for $\beta=1/3$ for SWCNT bundle interconnect. This can be explained that there are more metallic SWCNTs in a bundle when β increases.

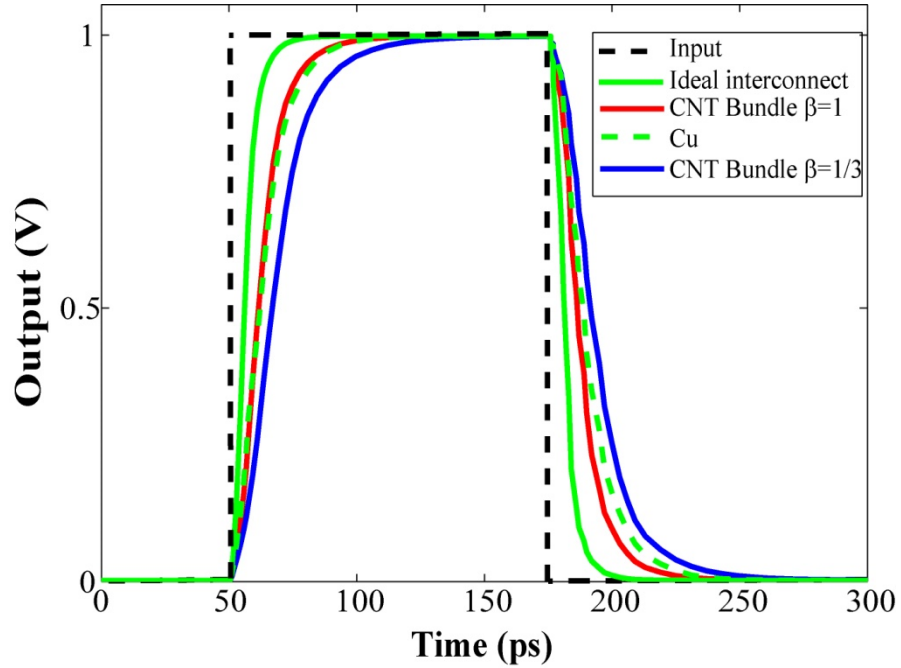


Figure 16 Input and output waveforms of a CNT-FET inverter pair with 0.1 μm length of different interconnect wires

Local interconnects are often used for connecting nearby gates or devices with lengths of the order of micrometers. Therefore, these have the smallest cross section and largest resistance per unit length compared to global interconnects.

Figure 17 shows output waveforms of a CNT-FET inverter pair using 10 μm SWCNT bundle interconnect and the comparison with the ideal interconnect ($RC=0$) and Cu interconnect wires. Input signal is a 15 MHz square wave pulse. The performance of SWCNT bundle ($\beta=1$) interconnect is better than Cu interconnect. While the delay of SWCNT bundle ($\beta=1/3$) interconnect is larger than the Cu interconnect due to contact resistance and relatively larger capacitance in a SWCNT bundle, the average delays are smaller when $\beta=1$ than $\beta=1/3$ for SWCNT bundle interconnect wires. This can also be explained that there are more metallic SWCNTs in a bundle when β increases.

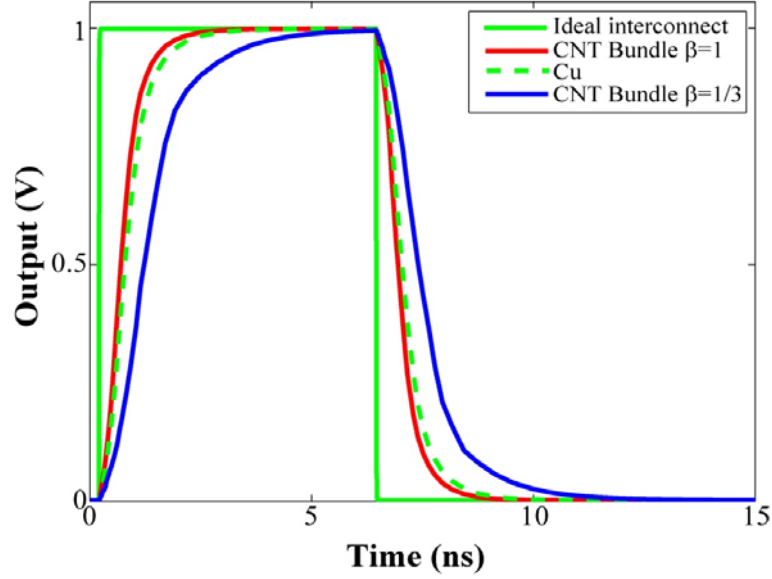


Figure 17 Output waveforms of a CNT-FET inverter pair with 10 μm length of different interconnect wires

Global interconnects have larger cross section and smaller resistivity. The lengths are of the order of hundred micrometers. Figure 18 shows output waveform of a CNT-FET inverter pair with 500 μm SWCNT bundle interconnect and comparison with the ideal interconnect ($RC=0$) and Cu interconnect wires. Here we have utilized the process parameters from the 2016 node, 22 nm technology and assumed 33 nm width and 87 nm height of a SWCNT bundle. It can be shown that there are nearly 1500 SWCNTs in the 33 nm (width) \times 87 nm (height) bundle following figure 12 assuming 1 nm diameter of a SWCNT. Input signal is a 2 MHz square wave pulse. The performance of SWCNT bundle ($\beta=1$) interconnect is much better than the Cu interconnect. While the delay of SWCNT bundle ($\beta=1/3$) interconnect is larger than the Cu interconnect, the average delays are smaller when $\beta=1$ than $\beta=1/3$ for SWCNT bundle interconnects. This explains further that there are more metallic SWCNTs in a bundle when β increases.

Our results show that the CNT-FET circuits can potentially operate up to 100 GHz. SWCNT bundle interconnect ($\beta=1$) has better performance than the Cu interconnect contrary to bundle with $\beta=1/3$. This results also compares well with the work of others showing that the SWCNT bundle interconnects have larger delay than Cu interconnects for $\beta=1/3$. The proportion of metallic nanotubes can also be potentially increased. The delay of SWCNT bundle interconnect can be smaller than that of Cu interconnect when β approaches to 1. The SWCNT bundle interconnect can potentially replace Cu interconnect in future CNT-FET circuits.

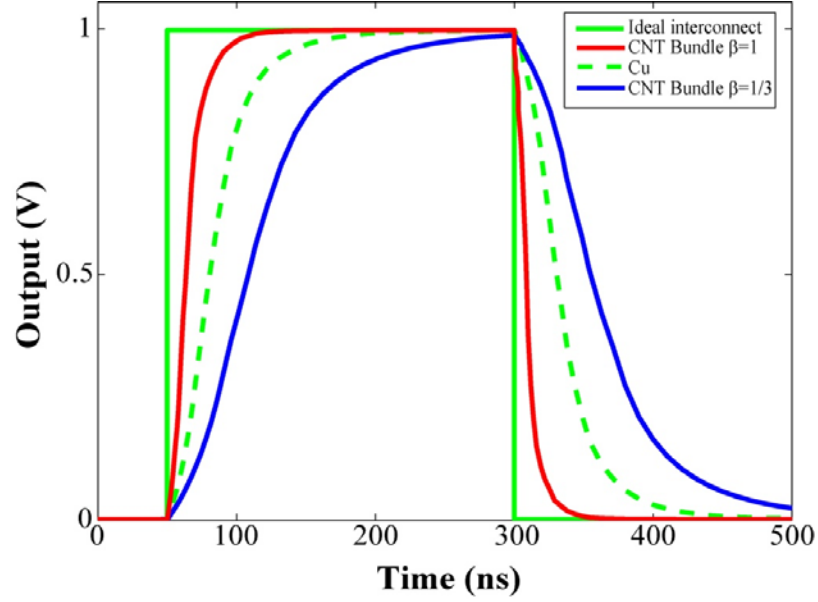


Figure 18 Output waveforms of a CNT-FET inverter pair with 500 μm length of different interconnect wires

In conclusion, static and dynamic model of CNT-FETs are introduced and models for SWCNT bundle interconnects are presented based on one-dimensional fluid model of SWCNTs. These models have been used to study the behavior of CNT-FET circuits such as ring oscillator and inverter pair and compared with the corresponding experimental behavior. The applicability of SWCNT bundle as interconnect wires in future design of integrated circuits has been explored theoretically and compared with the Cu interconnect wires for 22 nm technology node. Simulation results suggest that SWCNT bundle interconnect ($\beta=1$) can replace Cu interconnects as the technology scales down.

3.1.6 Multi-walled Carbon Nanotube (MWCNT) Interconnect Modeling

Previously, we proposed a model of SWCNT bundle interconnects, as shown in figure 19. The circuit can be further simplified as shown in figure 20. The capacitance, C_b has no effect on the circuit behavior and $\beta N_x \times C_E$ can be regarded as an electrostatic capacitance between SWCNT bundle and the ground plane.

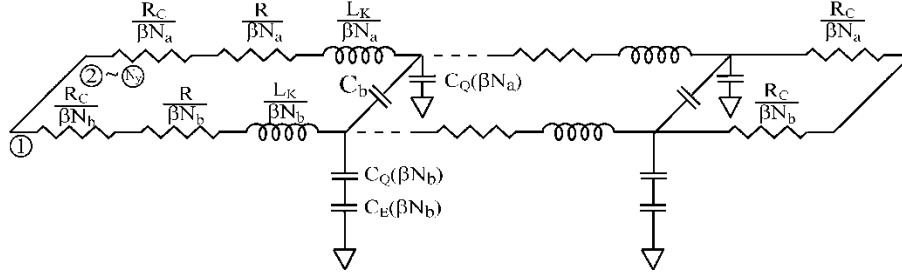


Figure 19 Equivalent circuit of a SWCNT bundle interconnect

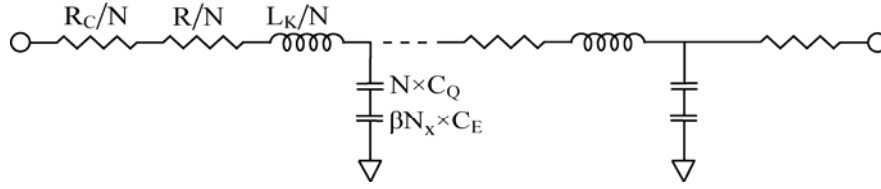


Figure 20 Simplified equivalent circuit of a SWCNT bundle interconnect

MWCNTs have diameters in a wide range of a few to hundreds of nanometers. It has been shown that all shells of MWCNT can conduct if they are properly connected to contacts and the contact resistance could reach tens of ohms, a much lower value than that of SWCNT. It has been shown that MWCNTs can have conductivities several times larger than that of Cu or SWCNT bundles for long length interconnects.

The number of shells in MWCNTs varies. The spacing between shells in a MWCNT corresponds to van der Waals distance between graphene layers in graphite, $\delta \approx 0.34$ nm. The number of metallic shells in a MWCNT can be calculated as follows:

$$M = \beta \left[1 + \frac{D_1 - D_N}{2\delta} \right], \quad (32)$$

where D_1 and D_N are the outermost and innermost shell diameters, respectively. The square bracket term is a floor function and the factor β is the ratio of metallic shells to total shells in a MWCNT. Statistically, one-third of the shells are going to be metallic and the rest semiconductor for $D_1 \leq 10$ nm. For $D_1 > 10$ nm, β increases due the interaction between adjacent shells for the MWCNT.

In one-dimensional fluid model, we regard the graphene sheet which is rolled to form a CNT is to be infinitesimally thin. The conduction electrons are then distributed over the lateral surface of the CNT cylinder shell and electrons are embedded in a rigid uniform positive charge background with a uniform surface number density. Thus, the motion of electrons is confined to the surface. Furthermore, electrical charge neutrality requires that in equilibrium the conduction electron charge density precisely cancels with that of the background positive ions. Since the van der Waals force between the carbon atoms in different shells in MWCNTs is negligible compared to valance

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band between the carbon atoms in the same shell, the one-dimensional fluid model can be applied to each shell of the MWCNT with modification because the electron-electron interaction in MWCNT is different from that in SWCNT, which means the parameter α needs to be recalculated.

In addition, two assumptions are made: the electrons can only move along the z-axis; all other fluid variables, such as the tangential component of the electric field to the nanotube surface are almost uniform in the cross section plane of the shells in MWCNT. These two assumptions are valid if both the nanotube length and the smallest wavelength of the electromagnetic field are much greater than the nanotube radius.

We assume that the velocity of these electrons equals the Fermi velocity. As a result, the kinetic energy is given by,

$$E_K = 4M \times \frac{1}{2} m v_F^2 \approx 7M \text{ eV} \quad (33)$$

There are two channels in each shell of MWCNT and two different spin electrons in each channel. So we consider that there are four electrons at the same point in each shell of MWCNT. We can then calculate the potential energy by moving these 4M electrons from ∞ to the same point of the MWCNT. We first consider moving every four electrons into one shell of the MWCNT. The potential energy can be obtained as follows:

$$E_P = \sum_{j=1}^M \left[\sum_{i=2}^4 (i-1) \frac{e^2}{2\pi\epsilon_0} \frac{1}{d_j} \right] = 6M \frac{e^2}{2\pi\epsilon_0} \sum_{j=1}^M \frac{1}{d_j}, \quad (34)$$

where d_j is diameter of shell number j .

We then consider moving all shells from ∞ to adjacent shells to construct a MWCNT. The potential energy can be calculated using following equation:

$$E_P = 6M \frac{e^2}{2\pi\epsilon_0} \sum_{j=1}^M \frac{1}{d_j} + \sum_{j=2}^M 4(j-1) \times \frac{4e^2}{2\pi\epsilon_0} \frac{1}{d_j} = 6M \frac{e^2}{2\pi\epsilon_0} \sum_{j=1}^M \frac{1}{d_j} + \frac{16e^2}{2\pi\epsilon_0} \sum_{j=2}^M \frac{j-1}{d_j}, \quad (35)$$

The parameter α for the MWCNT can be easily calculated. For example, if $D_1=10$ nm, $D_N=1$ nm and $\beta=1$ then $\alpha \approx 0.99$.

We can obtain an equation for each shell in a MWCNT,

$$\mathcal{E} = Ri + L_K \frac{\partial i}{\partial t} + \frac{1}{C_Q} \frac{\partial q}{\partial z}, \quad (36)$$

where $R \equiv L_K \text{sgn}(l)\nu$ is the resistance of each shell in a MWCNT per unit length. $L_K \equiv \pi\hbar/4e^2v_F$ is the kinetic inductance per unit length of each shell. $C_Q \equiv 1/L_K u_e^2$ is the quantum capacitance per unit length of each shell. $u_e = v_F/\sqrt{1-\alpha}$, is the thermodynamic speed of sound of the electron fluid under a neutral environment.

The magnetic inductance per unit length of each shell can also be calculated. In a SWCNT, magnetic inductance is neglected compared with kinetic inductance; therefore, it can also be neglected in each shell of a MWCNT.

The outermost shell shields inner shells from the ground plane; therefore, the electrostatic capacitance C_E does not exist in inner shells. However, there exists electrostatic capacitance, C_S between the neighboring metallic shells and its value is given by:

$$C_S = \frac{2\pi\epsilon_0}{\ln(D_i/D_j)}, \quad (37)$$

where ϵ_0 is the permittivity of vacuum, D_i and D_j are the diameters of the i^{th} and j^{th} metallic shells, respectively and $i < j$.

We assume that the outermost shell is metallic. In a recent work, we have derived an equivalent circuit of a metallic MWCNT interconnect as shown in figure 21. It is simplified as shown in figure 22 by considering that the RLC parts of all inner shells are identical. If we assume that there are no variation in distributed parameters, R and L_K then R and L_K are same for each shell. The potential across components of each shell in a MWCNT is equal. As a result, a simplified equivalent circuit of a MWCNT interconnect can be derived as shown as figure 23. R_C in figures 21-23 is the contact resistance and its ideal quantum value is 3.2 k Ω per shell.

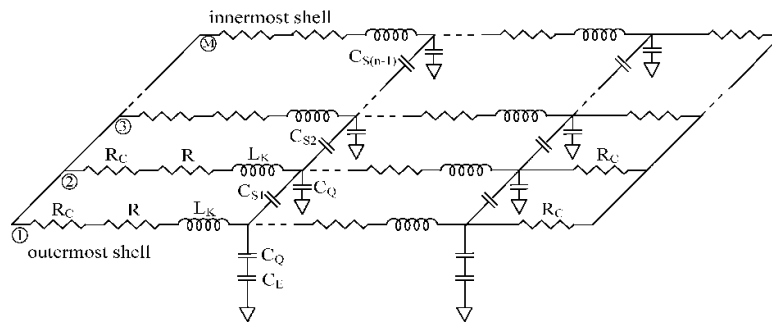


Figure 21 Equivalent circuit of a metallic MWCNT interconnect

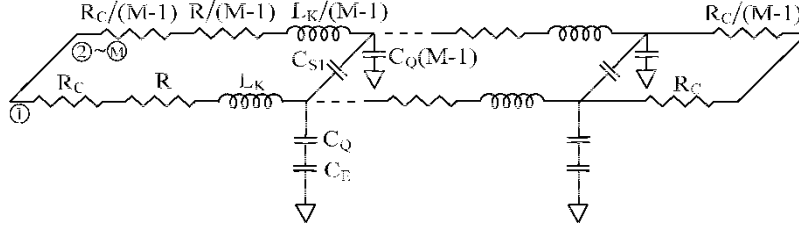


Figure 22 Simplified equivalent circuit of a metallic MWCNT interconnect

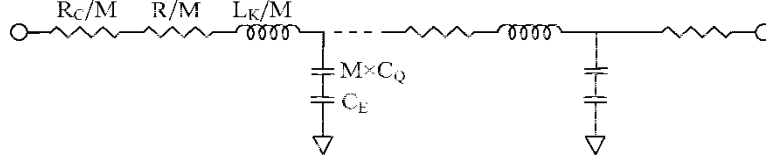


Figure 23 Simple equivalent circuit model of a metallic MWCNT interconnect

The values of C_E and C_Q are on same order. C_Q of all metallic shells is in parallel and then serial with C_E . As a result, C_Q can be neglected if M is large. Therefore, capacitance of MWCNT interconnect is smaller than that of SWCNT. In addition, the resistance and inductance of all metallic shells are parallel and M times smaller than that of SWCNT.

3.1.7 Performance of Carbon Nanotube Interconnects

We have extended one-dimensional fluid model for the modeling of MWCNT interconnects. To validate the model of MWCNT interconnect, we have compared the calculated resistance of MWCNT interconnect with the corresponding measured resistance from the work of Nihei et al. and Li et al. The results of the comparison of calculated and measured resistances are summarized in table 4.

Table 4 A comparison of calculated and measured resistances of MWCNT interconnects

References	MWCNT Physical Parameters				MWCNT Resistance (k Ω)	
	Length (μm)	D_1 (nm)	D_n (nm)	l_{mfp} (μm)	Measured	Our Model
Nihei et al.	2	10	3.8 8	<1	1.60	1.90
Li et al.	25	100	50	>25	0.035	0.042

CNT interconnects have great potential in extending the operation of circuits to higher speeds and frequencies. For applications requiring high frequencies where newer interconnect technologies and materials for interconnect are being explored, it is important to study two-port scattering parameters.. In this work, we focus on studying 2-port network scattering (S) parameters by CNT for interconnect applications on a chip.

Figure 24 shows the schematic of a 2-port network used in study of S-parameters. In figure 24, interconnect can be Cu or CNT and R_s is the terminal impedance. We have utilized the process parameters from the 2016 node (22 nm technology), assumed a 22 nm diameter of MWCNT of 22 nm width and 44 nm thickness of SWCNT bundle. If we assume diameter of the innermost shell in a MWCNT is to be 1 nm then there are nearly 30 shells in 22 nm MWCNT. If we assume diameter of a SWCNT in a bundle is to be 1 nm then there are nearly 500 SWCNTs in 22 nm (width) \times 44 nm (thickness) bundle following. The resistivity and capacitance of Cu were taken from International Technology Roadmap for Semiconductors (ITRS) 2007. The inductance of Cu wire can be modeled by the following equation ,

$$L = 2 \times 10^{-4} l \left(\ln \frac{2l}{w+t} + 0.5 + \frac{w+t}{3l} \right), \quad (38)$$

where l , w and t are the length, width and thickness of the Cu wire in micrometers.

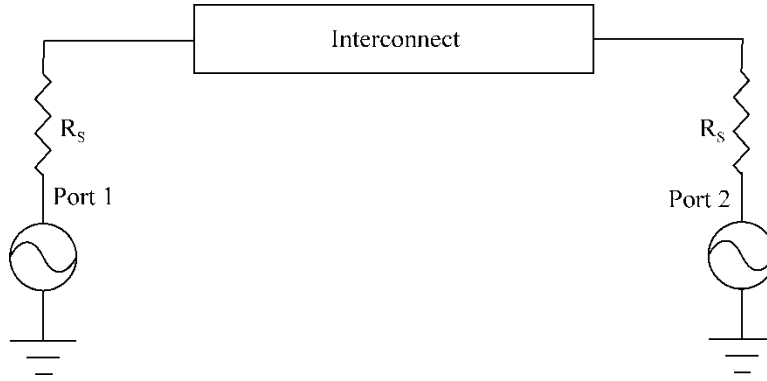


Figure 24 Schematic of a 2-port network of interconnects

In a recent work, we have used 2-port network analysis to compare S-parameters of SWCNT and Cu interconnects in 22 nm technology as shown in figures 25 and 26. In the analysis of SWCNT interconnect, the terminal impedance is assumed to be equal to its contact resistance; and in the analysis of Cu interconnect, the terminal impedance is assumed to be equal to its distributed resistance. Figures 25 and 26 show S_{21} and S_{11} parameters for Cu and SWCNT interconnects of 0.1, 1, 10 and 100 μm lengths. Since Cu has higher resistance and capacitance than that of SWCNT, single-walled CNT interconnect has larger 3dB bandwidth, higher transmission efficiency and lower reflection losses.

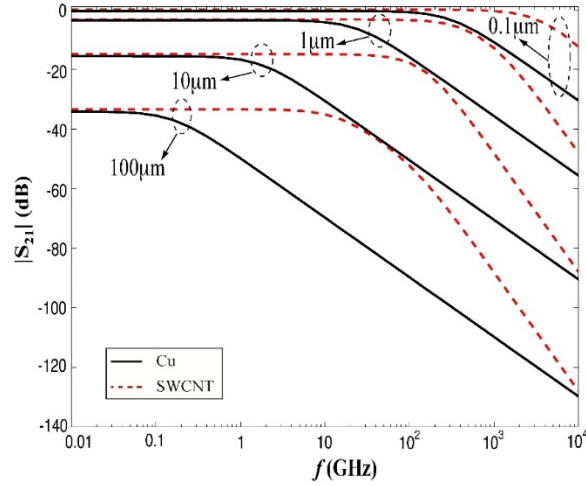


Figure 25 S_{21} (amplitude) versus frequency of different lengths SWCNT and Cu interconnects

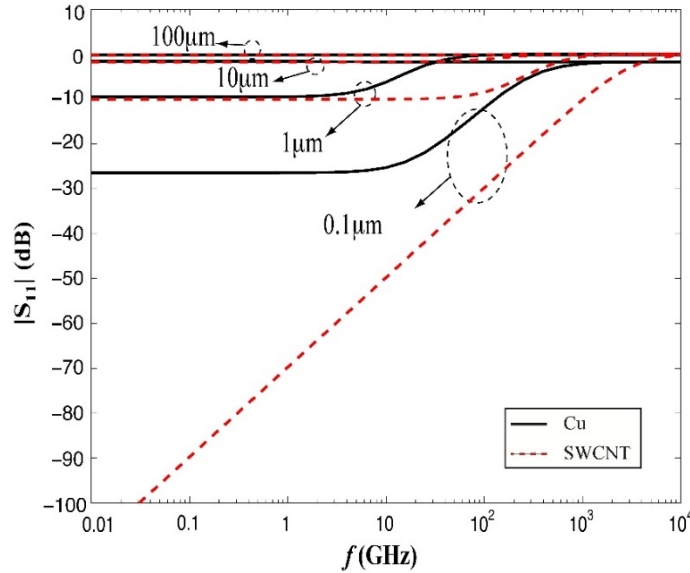


Figure 26 S_{11} (amplitude) versus frequency for different lengths SWCNT and Cu interconnects

SWCNT has very large contact resistance when used as interconnects, which limits its applications as interconnects for next generation integrated circuits. On the other hand MWCNT and CNT bundle give low contact resistance when used as the circuit interconnects. Contact resistance in MWCNT and SWCNT bundle, however, will depend on the number of shells or SWCNTs being metallic. It has been demonstrated experimentally that MWCNT can function as an interconnect wire on a chip and successfully transmit GHz digital signals from one transistor to another.

In table 5, modeling parameters of MWCNT are compared with the equivalent model parameters from the quantum theory. The difference is about 20 %. However, for large diameter, such as 100 nm diameter, the difference reaches to about 60%. According to quantum theory, the number of

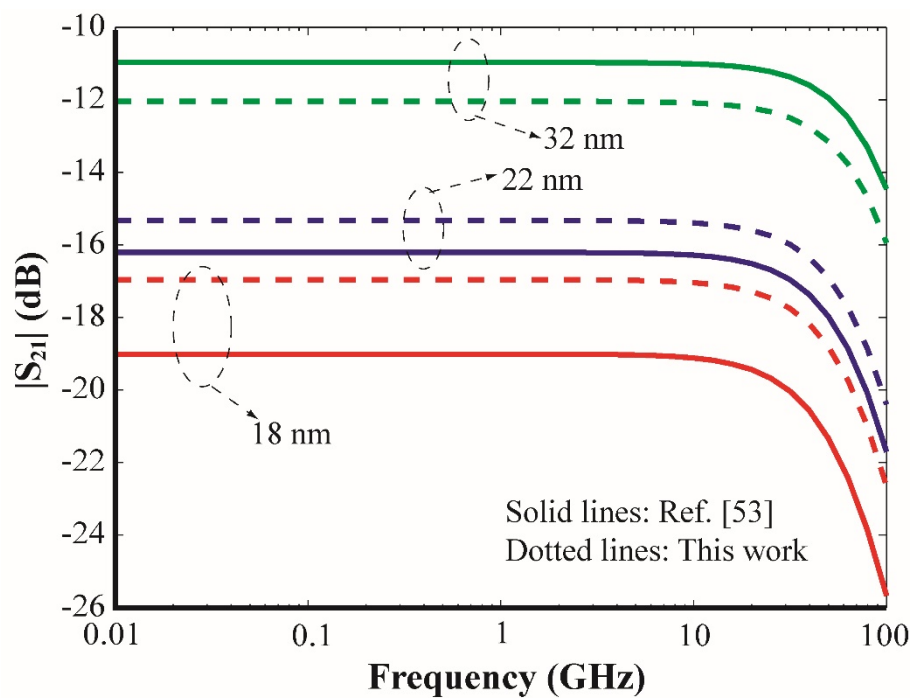
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channels increases significantly for large values of radius and the semiconducting shells start contributing significantly to the number of conducting channels since their axial conductivity increases with increasing radius. Our semi-classical one-dimensional fluid model assumes that the number of conducting channels in a single metallic CNT shell is fixed, 2, and 0 for semiconducting shells. Therefore, the difference in values of parameters between our model and quantum theory increases with the increase in diameter of MWCNTs. On the other hand, the parameter α decreases with the increase in diameter and quantum capacitance increases with the increase in diameter which is consistent with the quantum theory. As a result, the difference in values of parameters calculated from our model and quantum theory are not very large for small diameter MWCNTs. The electrostatic capacitance is dependent on the geometry of the structure, it is, thus, considered same for one-dimensional fluid model and quantum model.

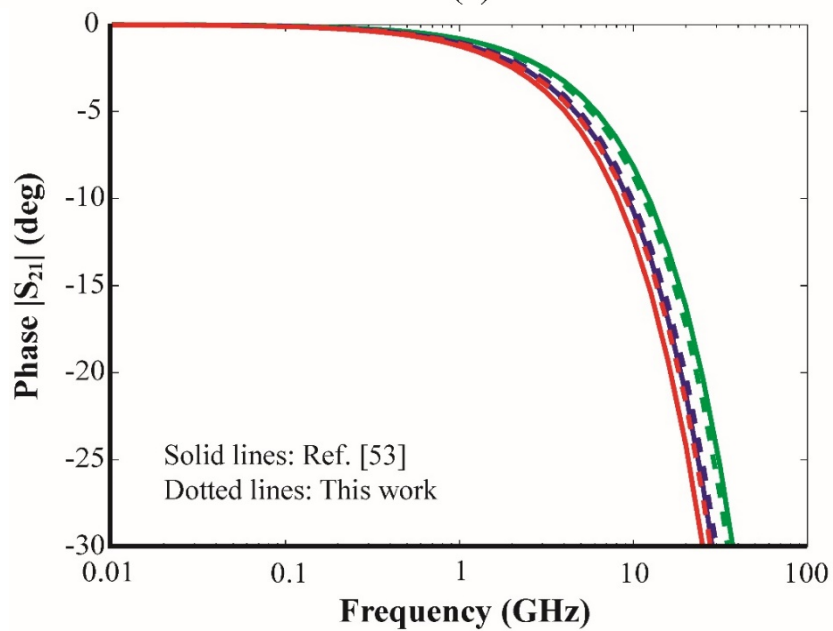
Table 5 A comparison of MWCNT interconnect model parameters

MWCNT Diameter (nm)	R_C (cal) $k\Omega$	R_C [24] $k\Omega$	R (Cal) $k\Omega/\mu m$	R [24] $k\Omega/\mu m$	L_K (cal) $nH/\mu m$	L_K [24] $nH/\mu m$	C_Q (cal) $aF/\mu m$	C_Q [24] $aF/\mu m$
18	0.81	1.05	0.81	1.05	1.00	1.31	1280	1160
20	0.65	0.78	0.65	0.78	0.80	0.97	1600	1566
22	0.65	0.72	0.65	0.72	0.80	0.90	1600	1682
25	0.54	0.55	0.54	0.55	0.67	0.68	1920	2228
28	0.46	0.43	0.46	0.43	0.57	0.53	2240	2844
32	0.40	0.34	0.40	0.34	0.50	0.42	2560	3622
90	0.16	0.06	0.16	0.06	0.21	0.08	11080	19208
100	0.11	0.04	0.11	0.04	0.17	0.05	17680	29845

Figures 27 and 28 show S_{21} and S_{11} parameters and comparison with the corresponding S-parameters for MWCNTs calculated using model parameters from the work of Li et al. In figures 27 and 28, solid lines shown by the reference 53 correspond to the work of Li et al. The dimensions used in comparison correspond to 18, 22 and 32 nm diameters of the outermost shells of MWCNTs which also correspond to nanometer CMOS technologies. The length of MWCNTs used in calculations is 10 μm . Terminal impedance is set equal to contact resistance and $D_I/D_N = 2$ and $\beta = 1/3$. The parameters, S_{21} and S_{11} in both models differs by about 6% corresponding to 18 nm diameter and it is less than 6% for 22 and 32 nm diameters. The phase difference is negligible within the 3dB bandwidths. It can, thus, be stated that the one-dimensional fluid model can be easily used in studying the performance of MWCNT interconnects.

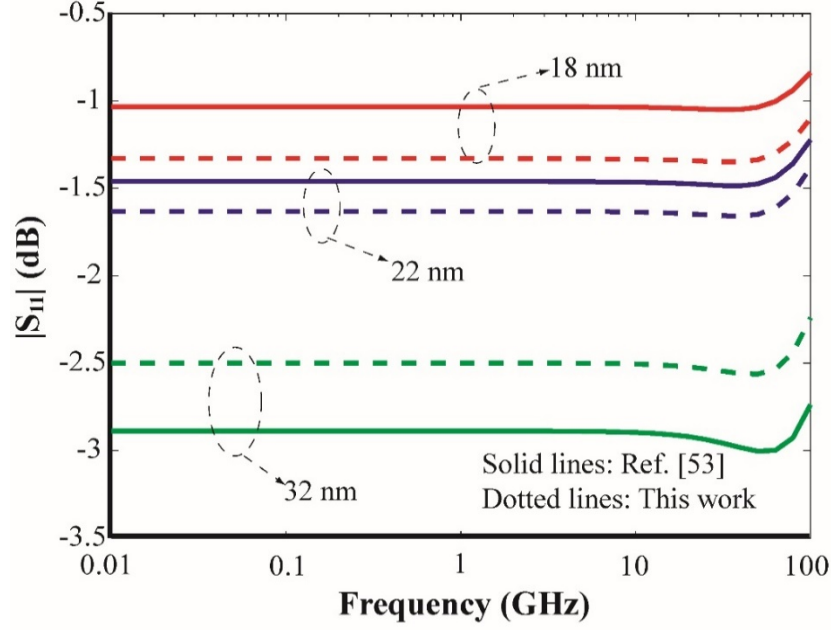


(a)

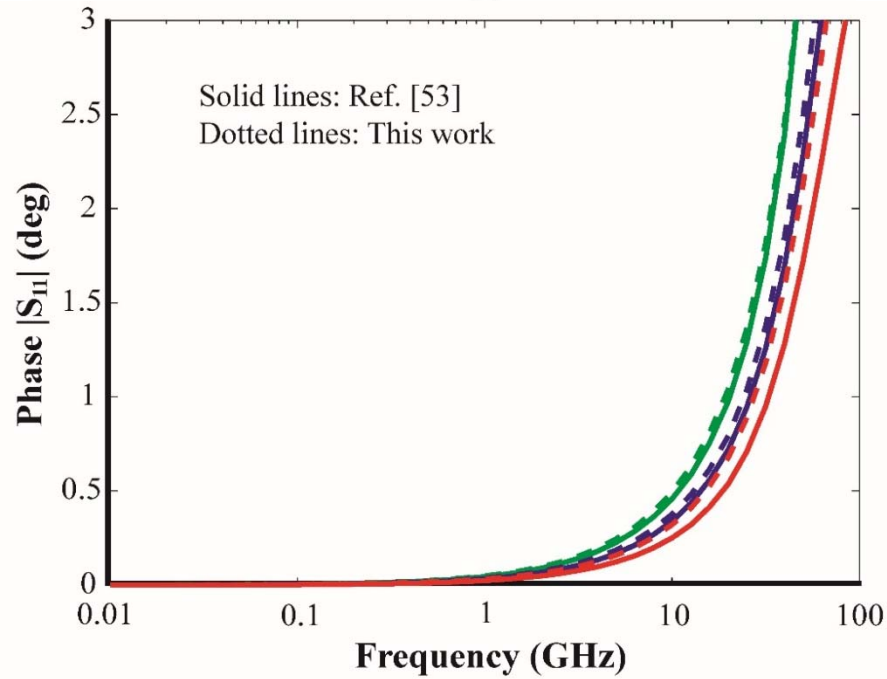


(b)

Figure 27 Comparison of S_{21} from our model and model for MWCNT interconnects: (a) amplitude and (b) phase



(a)



(b)

Figure 28 Comparison of S_{11} from our model and model for MWCNT interconnects: (a) amplitude and (b) phase

Figures 29 (a) and (b) show S_{21} and S_{11} parameters of MWCNT, SWCNT bundle and Cu interconnects of lengths corresponding to ballistic transport (1 μm), local interconnection (10 μm and 100 μm) and global interconnection (500 μm). For comparison, we choose $\beta = 1/3$ and 50 Ω terminal impedance, which is a typical impedance for high frequency transmission lines. For the

MWCNT and SWCNT bundle, the electrostatic capacitance depends upon the geometry of the structure and is approximately equal to that of Cu interconnects. Figure 29 (a) shows the 3-dB bandwidths for both the CNT and Cu interconnects. The transmission efficiency of both the CNT and Cu interconnects decreases with increasing lengths. However, Cu interconnect has a larger 3-dB bandwidth in comparison with CNT interconnects. This is because Cu has smaller inductance compared with CNT interconnects. It should also be noticed that the short length CNT interconnects still have over 100 GHz 3-dB bandwidth. Figure 29 (a) also shows large S_{21} for SWCNT bundle and MWCNT interconnects than that of the Cu interconnect. This is because SWCNT bundle and MWCNT have much smaller resistances. Furthermore SWCNT bundle has more connection channels than MWCNT, it has larger 3-dB bandwidth and S_{21} value, which means larger transmission efficiency. In figure 29 (b) for S_{11} parameters at frequencies less than 100 GHz, Cu interconnect has the largest reflection losses while SWCNT bundle interconnect has the least reflection losses. The results show that SWCNT bundle interconnect has better performance than the MWCNT interconnect. This can be explained that the number of SWCNTs in the bundle is larger than that of shells in the MWCNT of the same size. It can be shown that for 22 nm width of SWCNT bundle and MWCNT interconnects calculated number of SWCNTs in a bundle from $N = \beta(N_x N_y - [N_y/2])$ and the number of shells in a MWCNT are approximately 500 and 10, respectively. It means that there are more conducting channels in the bundle according to one-dimensional fluid model.

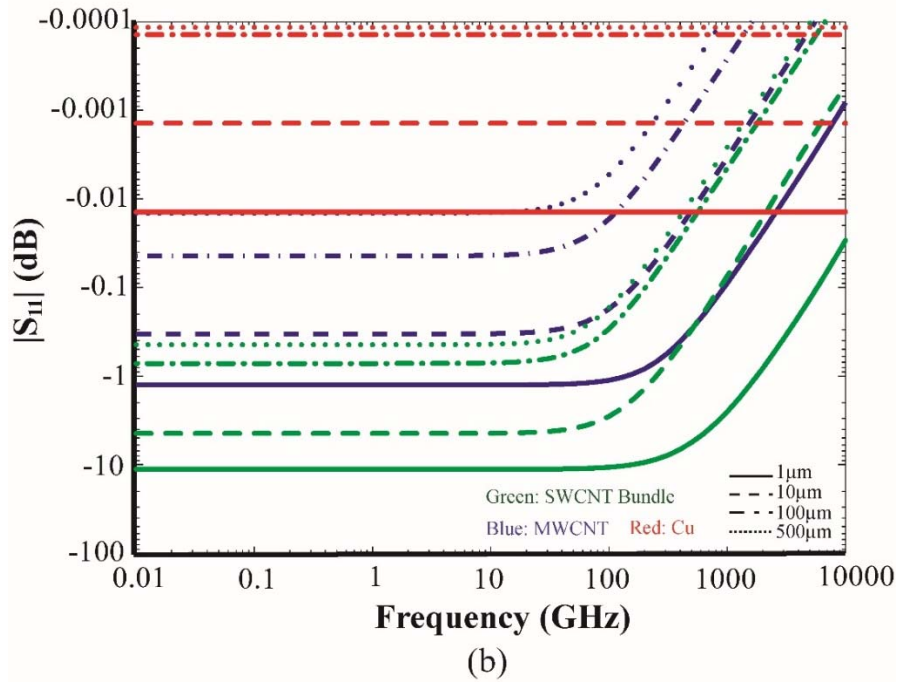
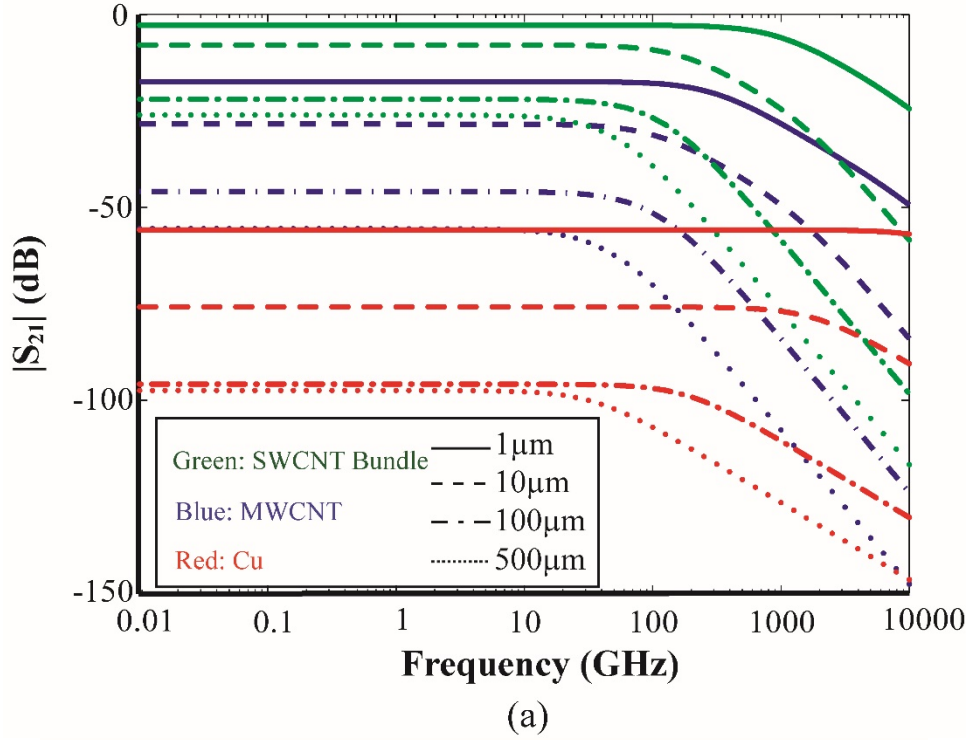


Figure 29 Calculated S-parameters of different interconnects: (a) S_{21} (amplitude) and (b) S_{11} (amplitude)

Recently, we have obtained an analytical solution for the current transport in CNT-FETs for the analysis and design of CNT-FET based integrated circuits. Based on our work, a dynamic model for CNT-FETs is obtained and Verilog-AMS language is used to predict static and dynamic characteristics of CNT-FETs and integrated circuits. Verilog-AMS requires less computational steps and easy to experiment with the developing model equations. In this work, Verilog-AMS is used to describe CNT-FET static and dynamic models and simulated CNT-FET circuits in Cadence/Spectre. Figure 30 shows the CNT-FET inverter pair at 1 V supply voltage. The interconnection can be Cu or MWCNT or SWCNT bundle. The delay analysis includes the CNT-FET models including the dynamic model developed by us.

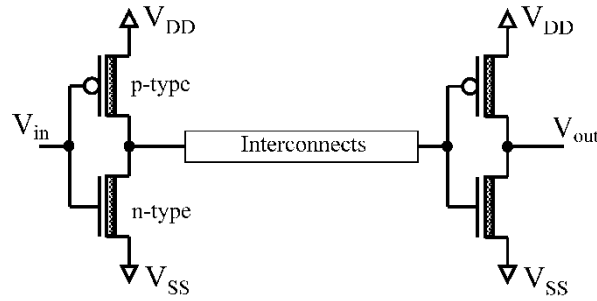


Figure 30 Inverter pair with interconnects.

Figure 31 shows transient response of a CNT-FET inverter interconnected with 10 μm long MWCNT and SWCNT bundle interconnection wires. Figure 31 also shows a comparison of transient response for an ideal interconnection (assuming direct connection) and Cu interconnection wire. Input signal is a 100 MHz square pulse. The propagation delays of MWCNT interconnects ($\beta = 1$ and $\beta = 1/3$) are close to ideal interconnect and are smaller than SWCNT bundle and Cu interconnects. As mentioned earlier, the number of SWCNTs in the bundle is larger than the number of shells in the MWCNT. Therefore, the resistance is smaller for the SWCNT bundle interconnect than that of the MWCNT. However, the capacitance of the SWCNT bundle interconnect is much larger than that of MWCNT. As a result, the propagation delay of MWCNT is smaller than that of the SWCNT bundle. The propagation delays are smaller for $\beta=1$ than for $\beta=1/3$ for both MWCNT and SWCNT bundle interconnects. This can be explained by the fact that there are more interconnect channels when β increases.

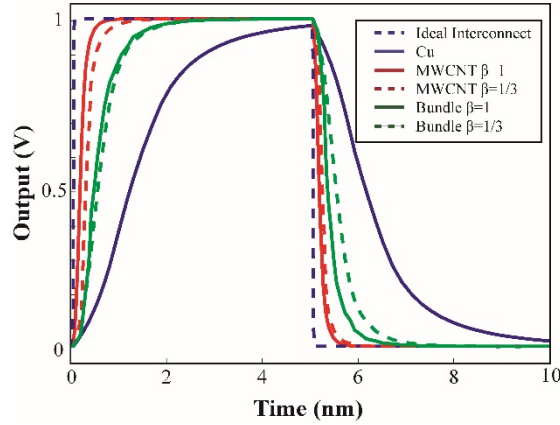


Figure 31 Output waveforms of an inverter pair with 10 μm length of different interconnect wires

3.1.8 Propagation Delays and Power Dissipation – Carbon Nanotube Interconnects and Comparison with Copper Interconnects

This part of the report summarizes propagation delays and power dissipation computation and comparison with the copper interconnects with reference to 22 nm CMOS technology node.

One of the advantages of CNT interconnect is its large mean free path, which is on the order of several microns as compared to ~ 40 nm for Cu at room temperature. It provides low resistivity and possible ballistic transport in short-length interconnects. In this work, we have also simulated a CNT-FET inverter pair with 1 μm Cu, MWCNT and SWCNT bundle interconnects using Cadence/Spectre. Local interconnects are often used for connecting nearby gates or devices with lengths on the order of micrometers. Therefore, these have the smallest cross section and largest resistance per unit length compared to global interconnects. We have utilized the process parameters from the 2016 node for 22 nm technology assuming 22 nm diameter of a MWCNT, 22 nm width and 44 nm thickness of a SWCNT bundle. Relatively global interconnects have larger cross section and smaller resistivity. The lengths are on the order of hundred micrometers. We have utilized the process parameters from the 2016 node of 22 nm technology assuming 33 nm diameter of a MWCNT, 33 nm width and 87 nm thickness of a SWCNT bundle. Simulations are performed for different lengths of Cu, MWCNT and SWCNT bundle interconnects corresponding to ballistic transport length (1 μm), local interconnects (10 μm , 100 μm) to global interconnects (500 μm). The results are shown in figure 32. Dependence of delay on interconnection length in figure 32 shows that the increase in delay for Cu interconnects is larger than that of MWCNT and SWCNT bundle interconnects. The delays of MWCNT interconnects ($\beta = 1$ and $\beta = 1/3$) are smaller than that of SWCNT bundle and Cu interconnects. The delays are smaller for $\beta = 1$ than for $\beta = 1/3$ for both MWCNT and SWCNT bundle interconnects and is due to more interconnect channels with increase in β .

Power dissipation is another challenge to next generation interconnects. We have simulated power dissipation for MWCNT and SWCNT bundle interconnects in 22 nm technology node and

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compared with the Cu wire interconnects. Table 6 summarizes power dissipation ratio of MWCNT and SWCNT bundle ($\beta = 1/3$ and $\beta = 1$) to Cu interconnect. CNT interconnects dissipates less power and especially for local interconnections. Maximum power dissipation in CNTs interconnections is no more than the 8% of the Cu interconnections.

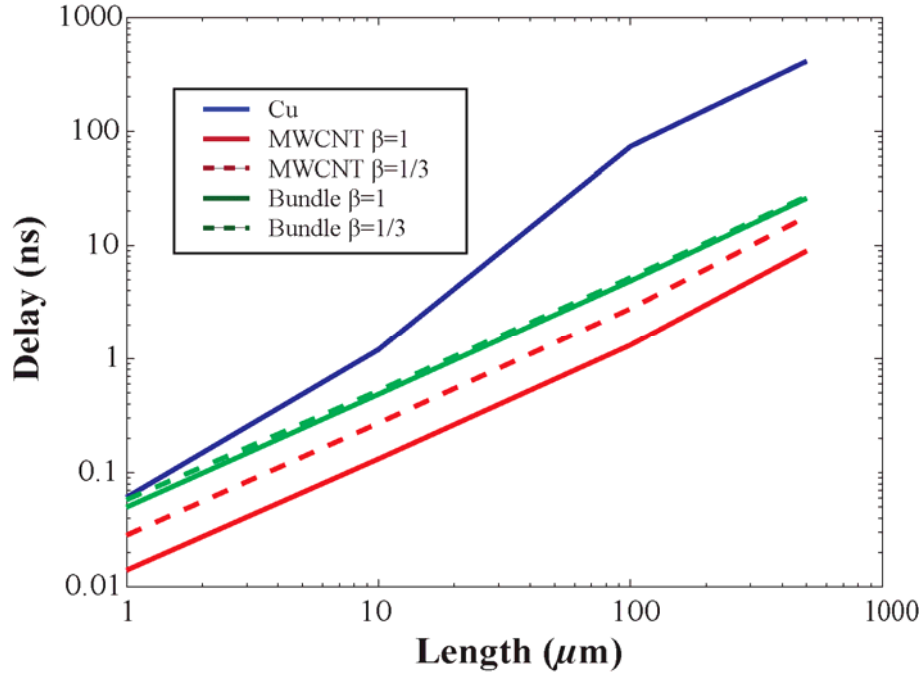


Figure 32 Propagation delays of interconnects of different lengths for 22 nm technology

Table 6 Power dissipation ratio of MWCNT and SWCNT bundle to Cu interconnects

Type of CNT	Normalized Power Dissipation (%)			
	Length (μm)			
	1	10	100	500
MWCNT ($\beta=1$)	0.070	0.065	0.339	1.422
MWCNT ($\beta=1/3$)	0.359	0.418	2.182	7.591
SWCNT Bundle ($\beta=1$)	0.011	0.015	0.079	0.137
SWCNT Bundle ($\beta=1/3$)	0.036	0.047	0.256	0.688

Note: Normalization parameter is the length of Cu (1, 10, 100 and 500 μm). The technology node is 22 nm.

With no special separation techniques, the metallic nanotubes are distributed with probability $\beta = 1/3$. While the proportion of metallic nanotubes can be potentially increased, the delays in MWCNT and SWCNT bundle interconnects can be further decreased with increase in β and

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approaching to 1. It is also noticed that with the increase in interconnection length, the delay of Cu interconnect increases faster than that of MWCNT and SWCNT bundle interconnects. For applications requiring small circuit delays MWCNT interconnects should be used due to smaller capacitances.

3.2 CNT-based Integrated Circuits

In the following, technical content are described in detail with focus on use of bundles of single-walled carbon nanotubes in design of LC voltage-controlled oscillators for use in phase-locked loop frequency synthesizer systems.

3.2.1 Carbon Nanotube Wire as an Inductor for use in Integrated Circuits – CMOS CNT-LC VCO Design using CNT Bundle Wire Inductor

Voltage controlled oscillators (VCOs) are widely used in radio frequency (RF) systems such as the rf transceivers which use phase-locked loops (PLLs) as frequency synthesizers. Digital cellular communication devices operating in 1-2 GHz range widely employ GHz VCOs. Commonly used VCO employ LC tuned circuit where quality factor of the inductor becomes crucial to the operation of the oscillator. In the past, inductor has been realized from bonding wires to retain the large quality factor. With shrinking device geometries and packaging requirements, on-chip inductors have been realized for the rf integrated circuits using Al and Cu metallization. A review on the design of CMOS voltage controlled oscillators and an on-chip 1.1 to 1.8 GHz VCO implementation in CMOS for use in rf integrated circuits is presented in the work of Salimath. However, achieving a high-Q inductor is still being researched.

The one-dimensional carbon nanotubes have been extensively researched for numerous applications including in electronics since its discovery in 1991. It has been demonstrated that the carbon nanotube wire is very likely to replace the Cu interconnect in sub-nanometer CMOS technologies. It has been shown that a CNT bundle wire has reduced skin effect compared to metal conductors such as the Cu and has a great promise for realization of high-Q on-chip inductors for rf integrated circuits. Physical design of a CNT-based spiral inductor has been also proposed. Several models of CNT based on-chip inductors have been presented in the literature.

Phase-locked loops operating in 1-2 GHz range suffer from phase noise which results in degradation in performance of rf systems where high frequency phase-locked loops are used. The LC VCO in PLL is the key contributor to the phase noise which uses a metallic wire on-chip integrated inductor. The resistive losses lower the inductor Q-factor in such LC VCO design. We proposed a new 2 GHz LC VCO design in TSMC 0.18 μm CMOS process using the CNT bundle wire as an inductor in LC tank circuit. We have applied our CNT interconnect model in a well-known π model to study the properties of CNT bundle wire on-chip inductors. Q-factors are calculated for the CNT bundle wire inductor and Cu wire inductor for comparison. It is shown from Cadence/Spectre simulation studies that the LC VCO using the CNT bundle inductor wire provide significant enhancement in oscillation frequency and phase noise in comparison to LC VCO using Cu inductor.

Figure 33 shows the cross-section of a SWCNT bundle. In figure 33, d is diameter of SWCNT, $\delta = 0.34 \text{ nm}$ is the spacing between the single-walled carbon nanotubes in the bundle and corresponds to the van der Waals distance between graphene layers in graphite. The distance between adjacent single-walled carbon nanotubes is $d_b = \delta + d$. Since van der Waals forces between carbon atoms in adjacent SWCNTs are negligible compared to valence band between carbon atoms in the SWCNT, influence of adjacent SWCNTs on transport of electrons in a SWCNT can be considered to be very small. Therefore, the one-dimensional fluid model can be applied to each of the SWCNT in the bundle considering electron-electron interaction.

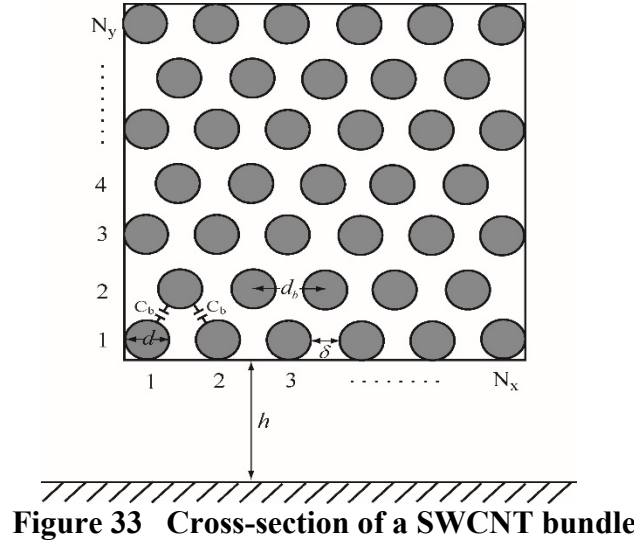


Figure 33 Cross-section of a SWCNT bundle

On-chip Inductor Modeling: The widely used π model is utilized to model the on-chip inductor as shown in figure 34.

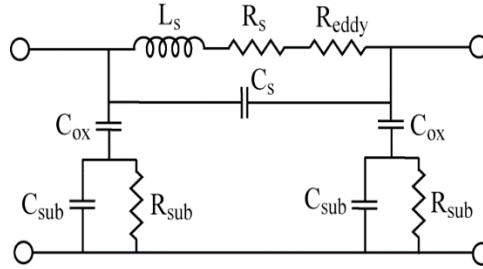


Figure 34 π model of on-chip inductor

In figure 34, L_s and R_s are the series inductance and resistance of interconnects, respectively. The series capacitance (C_s), oxide layer capacitance (C_{ox}), substrate resistance (R_{sub}) and substrate capacitance (C_{sub}) in figure 34 are calculated by using the modeling techniques based on the total length of the inductor.

The performance of CNT bundle inductors are analyzed and compared to that of Cu inductors. We studied the utilization of CNT bundle inductor in $0.18 \mu\text{m}$ CMOS technology. The inductor considered is a 4.5 turn planar spiral inductor, which has the outermost diameter, $D_{out} = 250 \mu\text{m}$, conductor width, $W = 15 \mu\text{m}$, conductor thickness, $t = 2 \mu\text{m}$, conductor spacing, $S = 1.5 \mu\text{m}$, oxide and substrate thicknesses of 4 nm and $300 \mu\text{m}$, respectively. The Q factor analysis results are shown in figure 35 for $L = 6 \text{ nH}$. The maximum Q factor of CNT bundle ($\beta=1$) wire inductor can be $\sim 600\%$ higher than that of the Cu wire inductor. This significant enhancement in Q factor arises not only because of the lower resistance of CNTs but also because the skin effect in CNT interconnects is negligible.

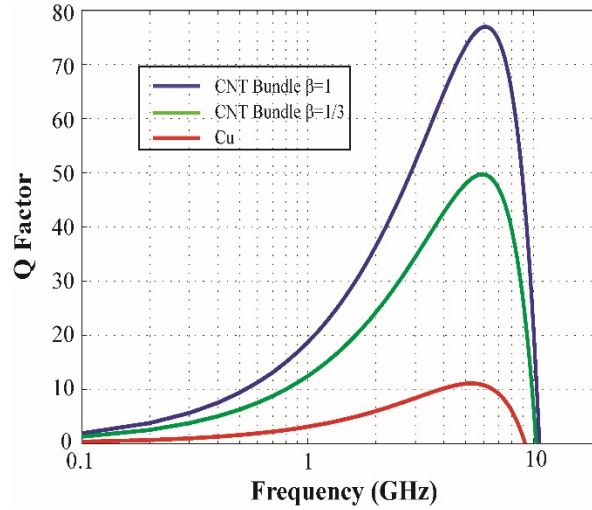


Figure 35 Q-factor of inductors based on CNT and Cu wires

LC Voltage-Controlled Oscillator (VCO): An inductor capacitor (LC) VCO consists of three components: LC tank, tail bias transistor and cross-coupled differential pair. LC tank is made by an inductor and a capacitor connected in cascade or in parallel. The resonance frequency of LC tank circuit is given by, $f_0 = \frac{1}{2\pi\sqrt{LC}}$. When the tank is a purely resistive the phase of the impedance is zero. Below the resonance frequency, the LC circuit is capacitive and above the resonance frequency, it is inductive.

In this work, we proposed design of a 2 GHz LC VCO in TSMC $0.18\mu\text{m}$ CMOS process where an inductor in LC tank circuit is realized from a CNT bundle wire. Figure 36 shows the circuit diagram of a complementary cross-coupled differential LC oscillator circuit with tail current. The symmetrical design of the VCO gives good phase noise performance and large voltage swing. The value of the inductor is chosen to be 6 nH for the physical dimensions of SWCNT bundle and Cu wires described earlier. The varactor in the circuit of figure 36 is implemented from an nMOSFET with source and drain tied together. The C-V curve of the varactor is shown in figure 37. The voltage-controlled capacitance range is from 200 fF to 2.2 pF which makes the LC VCO to oscillate from 1.6 GHz to 3.3 GHz .

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Figure 38 shows the plot of LC VCO oscillation frequency versus control voltage for an inductor with no losses (ideal), CNT bundle ($\beta = 1$, $1/3$) wire inductors and a Cu wire inductor. Here, β is the probability factor characterizing the SWCNT being metallic in a bundle. CMOS LC VCO with a CNT bundle ($\beta = 1/3$) wire inductor oscillates between $1.3 - 2.6 \text{ GHz}$ which is higher in comparison to an oscillation frequency range, $1.1 - 2.4 \text{ GHz}$ of LC VCO with a Cu wire inductor. It is also shown that VCO with a CNT bundle wire inductor ($\beta = 1$) has the oscillating frequency higher than that of a Cu wire inductor. For example, oscillation frequency of a CNT bundle ($\beta = 1$) wire inductor is higher by $\sim 10\%$ at 1.2 V than that with the Cu wire inductor.

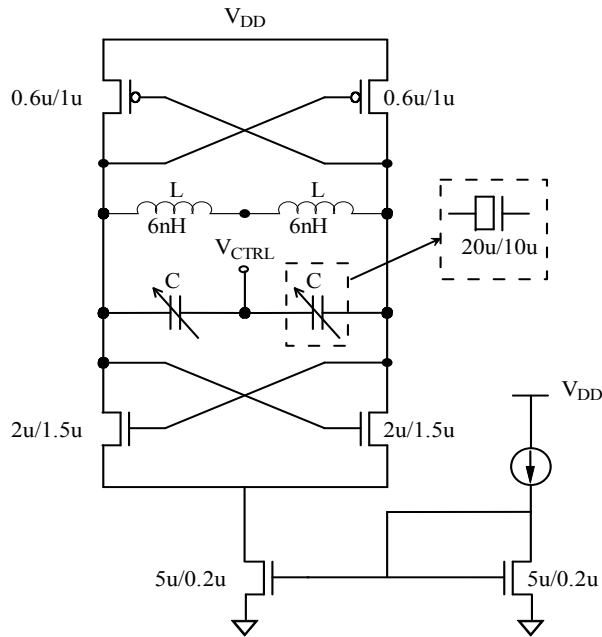


Figure 36 Circuit diagram of a LC VCO

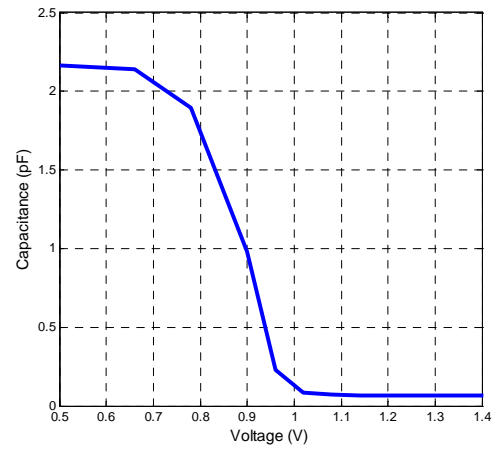


Figure 37 C-V curve of a varactor

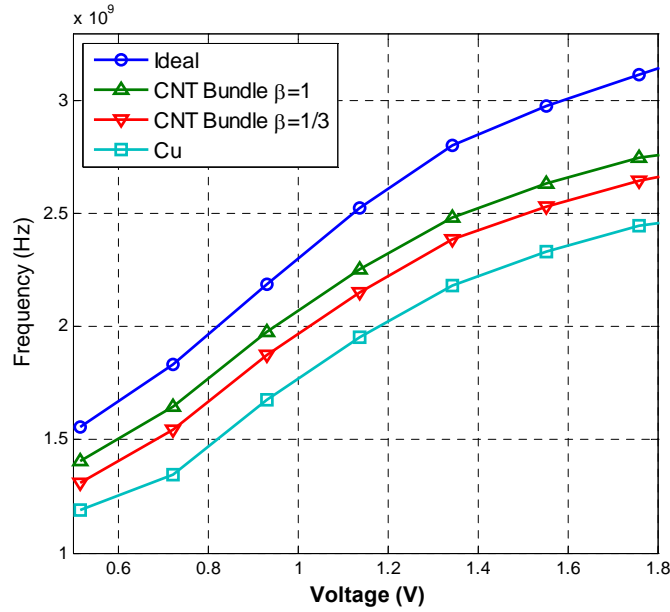


Figure 38 VCO oscillation frequency versus control voltage with different inductors.

At 1.2 V control voltage, the calculated Q factor of the Cu inductor from figure 35 is 7 and Q factors of CNT bundle wire inductors are 38 (for $\beta = 1$) and 26 (for $\beta = 1/3$). The oscillating frequency is higher in VCO with the CNT bundle wire inductors for $\beta = 1$ than that of $\beta = 1/3$.

The noise is modeled by using the phase noise density equation,

$$L(\Delta f) = \left(\frac{1}{8Q^2} \right) \left(\frac{FkT}{P} \right) \left(\frac{f_0}{\Delta f} \right)^2, \quad (39)$$

where k is the Boltzmann's constant, T is the temperature in $^{\circ}\text{K}$, P is the output power, F is the noise factor, Q is the quality factor of the LC tank circuit, f_0 is the oscillation frequency and Δf is the offset frequency from f_0 .

Figure 39 shows the phase noise of the LC VCO at 2 GHz tuning frequency. The VCO phase noise using an inductor with no losses (ideal) is -70dBc/Hz at 10 kHz offset frequency from the carrier and -123dBc/Hz at 10MHz offset frequency from the carrier. The VCO with CNT bundle wire inductors has about 10 dBc/Hz smaller phase noise than that with Cu wire inductors. Moreover, at this 2 GHz tuning frequency, the calculated Q factor of a Cu wire inductor from the figure 35 is 7 and Q factor of CNT bundle wire inductors are 36 (for $\beta = 1$) and 25 (for $\beta = 1/3$). The phase noise is smaller in VCO with CNT bundle wire inductors for $\beta = 1$ than for $\beta = 1/3$.

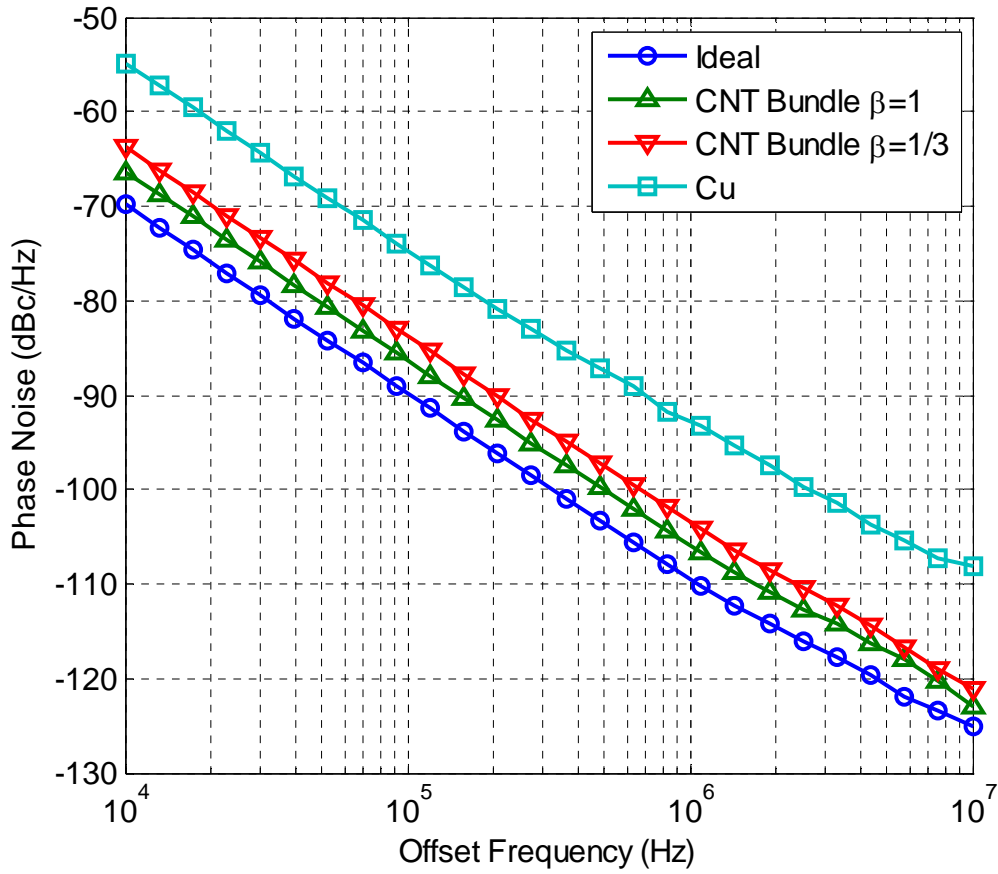


Figure 39 VCO phase noise versus offset frequency

3.2.2 Conclusion

We have utilized our CNT bundle interconnects model in a widely used π model to study the performances of CNT bundle wire inductors and compared them with Cu wire inductors. The theoretical results show that the Q factors of CNT bundle wire inductors are much higher than that of a Cu wire inductor. This is mainly due to much lower resistance of the CNT bundle wire and negligible skin effect in carbon nanotubes at higher frequencies. The application of a CNT bundle wire inductor in LC VCO is also studied and the simulations from Cadence/Spectre show that VCOs with CNT bundle wire inductors have significantly improved performances such as the higher oscillation frequency, reduced phase noise due to their smaller resistances and higher Q factors. The multi-walled CNT wire as an inductor design for use in integrated circuit is currently being explored and will be a part of future interim reports.

Fabrication of spiral CNT inductors and on-chip integration with current CMOS process face finding the solutions of intermediate processing steps. It is beyond the scope of the present work to describe experimental realization of LC VCO with on-chip CNT wire inductor.

3.3 Bio and Chemical Sensing

Single-walled carbon nanotube (SWNT) graphite cylinders are composed of surface atoms. Because of their size, large surface area and hollow geometrical shape, carbon nanotubes are the best-suited materials for gas absorption, storage and molecular filtering. Many carbon materials are known to possess excellent molecular adsorption properties. Carbon nanotube is among one of the materials, which has exhibited significant changes in its electronic properties when subjected to molecular adsorbates. The unique structure and sensitivity to molecular adsorbates have resulted in use of carbon nanotubes for bio- and chemical sensing applications. Both conductance and capacitance based CNT-sensors have been developed for detecting traces of a wide range of chemical vapors and gases including traces of nerve agents and explosives. In this section, we give a brief description of CNT-FET based sensors for bio- and chemical sensing applications and we have shown how our presented model equations can be used for interpreting the effect on the I-V characteristics when CNT-FETs are exposed to a bio-molecular trigger environment.

3.3.1 Carbon Nanotube Sensing Mechanism

Snow, et al. have provided an excellent review of chemical vapor detection using single-walled carbon nanotubes. Collins et al. have shown that electronic properties of SWNTs are extremely sensitive to oxygen or air and dramatically changes the electrical resistance, thermoelectric power and local density of states, $N(E)$. Atashbar et al. have fabricated a simple SWNT conductance based sensor for the detection of streptavidin and mouse monoclonal immunoglobulin G (IgG) antibody. Figure 40 shows the schematic representation of the bio-sensor for detecting (IgG).

Carbon nanotubes have been used for the detection of deoxyribonucleic acid (DNA). The detection of DNA is important to the detection of infectious agents, drug delivery and warning against bio-warfare agents. Tang et al. have developed a fully electronic DNA sensor based on CNT-FETs. Figure 41(a) shows the optical image of the central region of a single sensor chip with four SWNT-FETs. Figure 41(b) shows the concept illustration of a single CNT-FET during electrical measurements.

After mercaptohexanol (MCH) attachment, I- V_g curves are taken by a sweeping silicon backgate. I- V_g characteristics show the device conductivity due to change in alignment in energy level before and after DNA hybridization as shown in figure 42.

Snow et al., have experimented with a SWNT network type sensor, a cross-section of which is shown in figure 43. The SWNT sensor of the type shown in figure 43 can be used both as a conductance sensor and capacitive sensor.

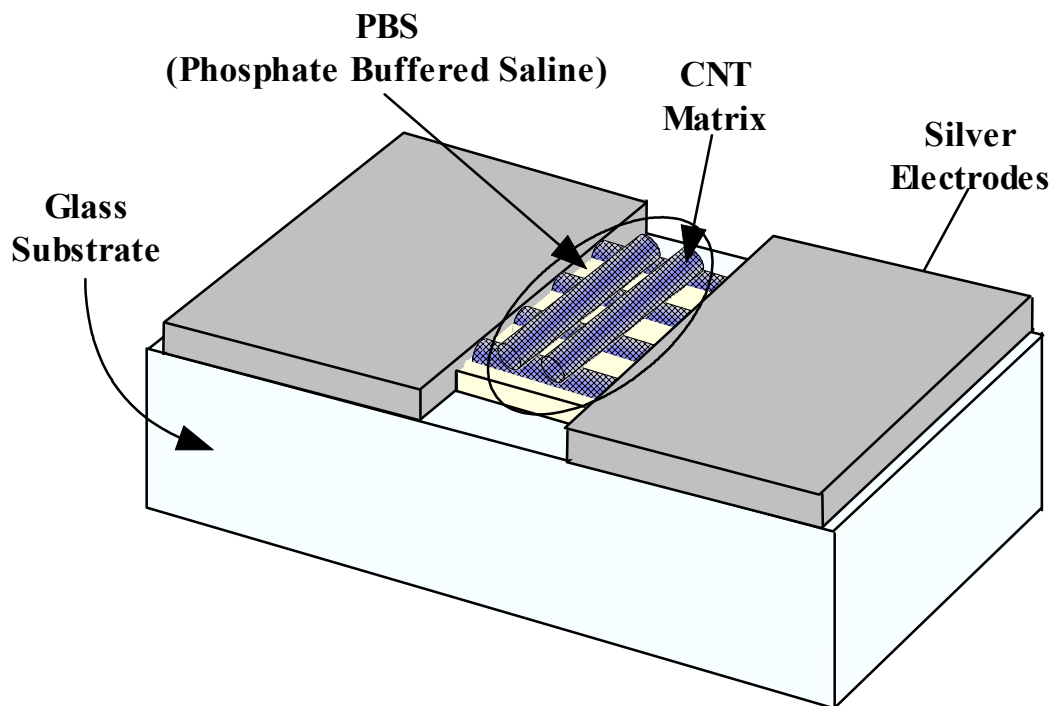


Figure 40 Simple SWNT conductance-based bio-sensor for detecting 10 μ l IgG antibody

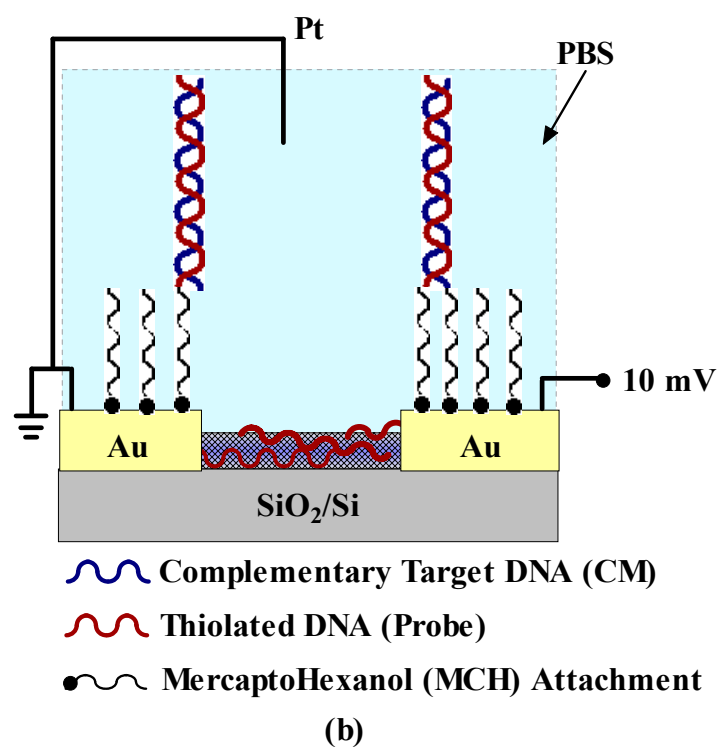
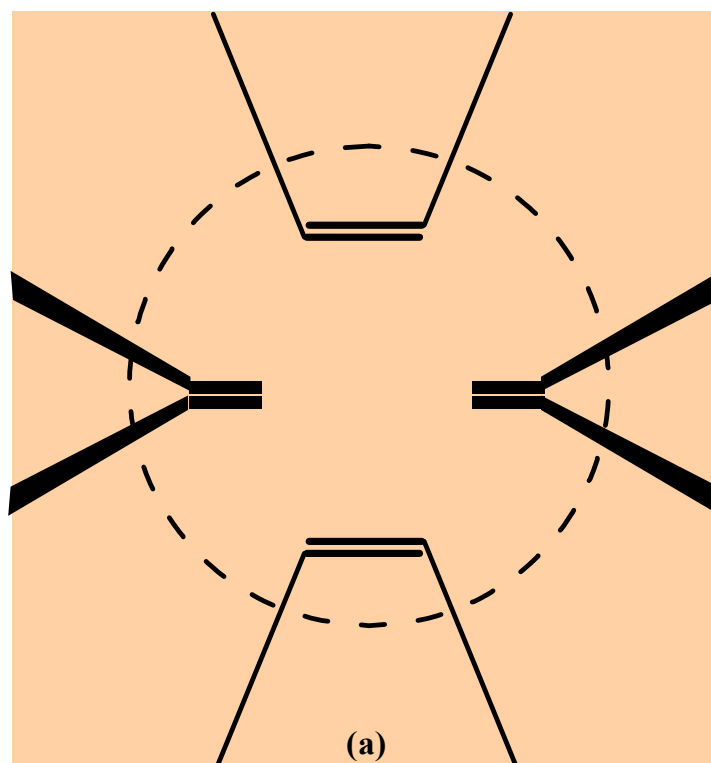


Figure 41 (a) Single sensor chip with four SWNT-FETs and (b) illustration of a single SWNT-FET during electrical measurements

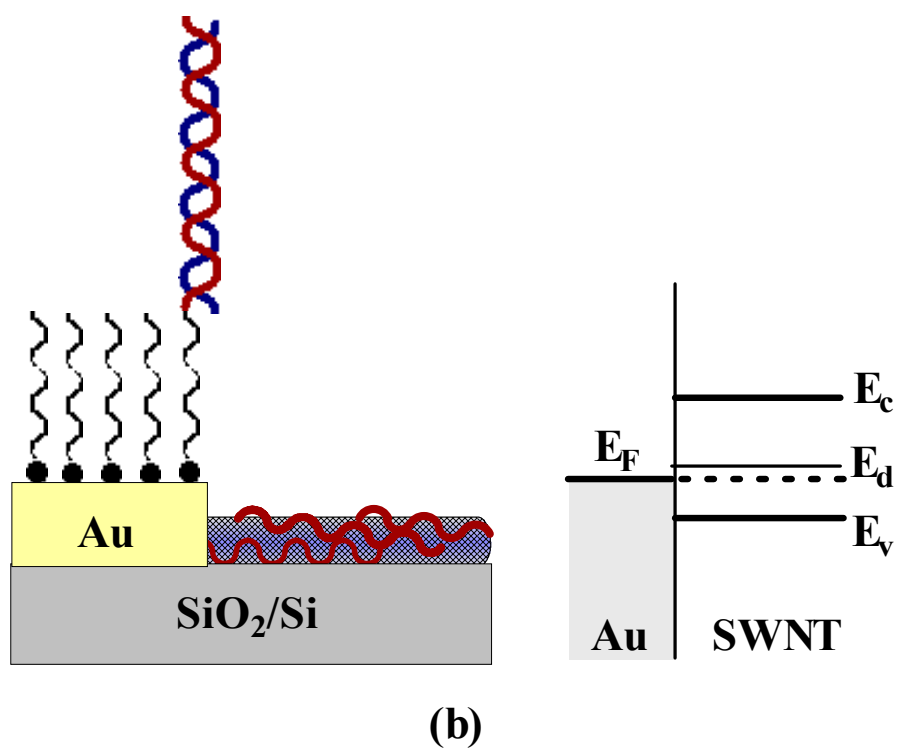
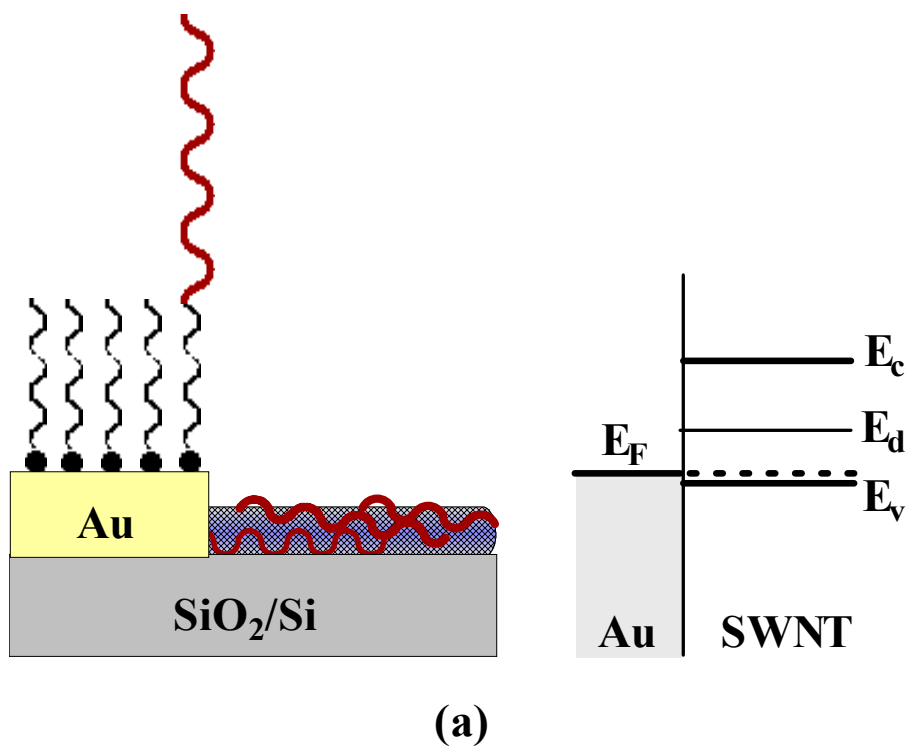


Figure 42 Energy level alignment between Au and SWNT (a) before and (b) after DNA hybridization

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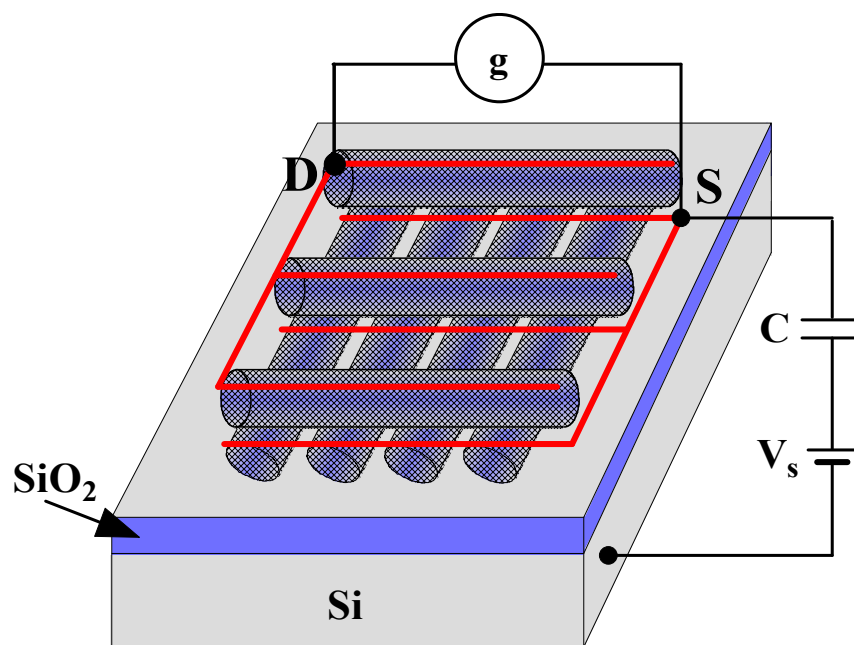


Figure 43 Cross-section of a SWNT network sensor

3.3.2 Summary

Semiconducting SWNT molecular wires and SWNT-FET based sensors are promising compact ultra-sensitive and low power advanced miniaturized sensors in comparison to conventional sensors. Their ability to operate at room temperature and detect traces of bio-warfare agents and chemical agents (nerve agents, blister agents and explosives) show a great promise for defense and homeland security applications. The presented research on current transport modeling can be easily applied in providing explanations to reactions taking place in the CNT and CNT-FET sensors when exposed to traces of bio- and chemical agents at a molecular level. Carbon nanotubes field effect transistors are therefore very promising devices for use in bio-sensing applications.

3.4 A Thermal Model for Carbon Nanotube Interconnects

3.4.1 Introduction

The current complementary metal oxide semiconductor (CMOS) technology in nm- and sub-nm node for VLSI is facing challenges due to performance limitation of Cu/low-k dielectric material as an interconnection, because of increased resistivity of Cu, electromigration and void formation. Many alternatives to Cu interconnection in nm technology node have been proposed in the literature, including optical interconnects. The 1D carbon nanotubes and graphene nanoribbons are found to be very promising alternatives to current Cu interconnects for use in nm-CMOS technology. Early discovery of carbon nanotubes in 1991 by Iijima and its excellent electrical, mechanical and thermal properties and established synthesis techniques, have led to major R&D efforts in integrating carbon nanotubes in CMOS processes, whereas graphene nanoribbon as a possible substitute for Cu interconnect is also evolving.

Though carbon nanotube has high thermal conductivity, it has been observed experimentally that the conducting carbon nanotube breaks down due to Joule heating which thus limits its current density. Notable work has been done in electrical modeling of carbon nanotube as an interconnect material, substituting Cu/low-k from quantum and classical considerations. Recently, we have conducted exhaustive studies on single-wall carbon nanotube interconnect from one-dimensional fluid model and included electron-electron repulsive interaction and extended to multi-wall carbon nanotubes and bundles of single-wall carbon nanotubes. Thermal effects in VLSI interconnect limits the current density and there have been problems of breakdown in carbon nanotubes due to resistive heating. Santini has done exhaustive experimental studies on Joule heating-induced breakdown of carbon nanotube interconnects and attribute to the defect sites. Naeemi and Meindl have studied temperature coefficient of resistance of single- and multi-wall carbon nanotube interconnects and related to various electron-phonon scattering mechanisms. In this work, we have examined the problem of Joule heating in carbon nanotube interconnects based on one-dimensional fluid model of electronic transport considering various scattering mechanisms and studied the temperature distribution across the length of the nanotube and scattering parameters.

3.4.2 Electrical and Thermal Transport Model

The conducting single-wall, multi-wall and bundle of single-wall carbon nanotube have been considered for possible replacement of Cu/low-k dielectric interconnects used in current CMOS technology depending upon the type of the interconnect, such as whether local or global. In the present work, we have considered Joule heating in a metallic single-wall carbon nanotube for better understanding of breakdown and also for analytical simplicity.

In our earlier work, we have made modification in two-dimensional fluid model and included electron-electron repulsive interaction and considered distribution of conduction electrons on the lateral surface of SWCNT cylindrical shell. The analysis reduces to semi-classical one-dimensional fluid model. The SWCNT is a two-dimensional graphene sheet rolled to form a cylindrical nanotube of infinitesimally thin layer. Thus, conduction electrons are distributed on the lateral surface of the SWCNT and motion of electrons is confined to the surface. As the diameter of CNT is very small we can also assume that the electron is confined in one-dimensional space. We can assume that cloud of electrons is moving across the surface of the nanotube. Figure 44 shows a structure of a single-wall carbon nanotube.

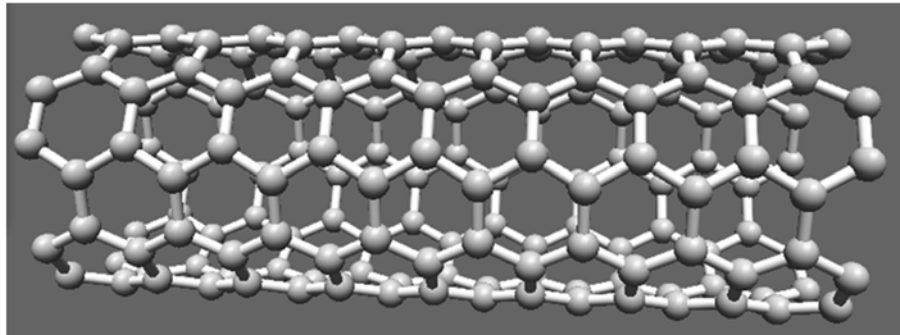


Figure 44 Single wall carbon nanotube

The motion of electrons across the SWCNT in a 1D fluid model can be described by the following equation ,

$$\frac{\partial j(z,t)}{\partial t} + \nu j + u_e^2 \frac{\partial \sigma(z,t)}{\partial z} = \frac{e^2 n_0}{m} (1 - \alpha) \varepsilon_z \quad (40)$$

where j is the current density, m is effective mass of an electron, n_0 is equilibrium three-dimensional electron density and σ is conductivity. Electron-electron repulsion factor is described by α . The thermodynamic speed of sound is u_e ; e is electronic charge, ε_z is electric field and ν is relaxation frequency of electron. Equation 40 describes the relation between an electric field and the current density.

We have modified the relaxation frequency (ν) in equation 40 considering the effective mean free path as follows,

$$\nu = \frac{v_F}{\lambda_{eff}} \quad (41)$$

In equation 41, v_F is Fermi velocity of electron and λ_{eff} is effective mean free path of an electron which accounts for acoustic and optical phonon scattering mechanism responsible for increased resistance of the interconnect. The spontaneous scattering length for emitting an optical phonon (λ_{op}) and acoustic phonon (λ_{ac}) can be estimated as follows,

$$\lambda_{op} = 56.4D \quad (42)$$

$$\lambda_{ac} = \frac{400.46 * 10^3 D}{T} \quad (43)$$

These two scattering lengths depend on diameter of the carbon nanotube (D) and surrounding temperature (T). The scattering length due to optical phonon absorption, $\lambda_{op,abs}$ has been modeled by the following equation,

$$\lambda_{op,abs} = \lambda_{op} \frac{N_{op}(300) + 1}{N_{op}(T)} \quad (44)$$

In equation 44, N_{op} describes the optical phonon occupation which can be calculated from Bose-Einstein statistics given by,

$$N_{op} = \frac{1}{\exp\left(\frac{\hbar\omega_{op}}{K_B T}\right) - 1} \quad (45)$$

where $\hbar\omega_{op}$ is optical phonon energy and its typical value varies from 0.16 eV to 0.20 eV. In our work, we have taken this value as 0.16 eV. Occupancy function of optical phonon increases as

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temperature increases which eventually decreases optical phonon absorption component ($\lambda_{op,abs}$) of electron mean free path. Optical phonon emission process has two components, one is for the absorbed energy ($\lambda_{op,ems}^{abs}$) and another ($\lambda_{op,ems}^{fld}$) is for the electric field across the SWCNT length. Both of these components are expressed as follows,

$$\lambda_{op,ems}^{abs} = \lambda_{op,abs} + \frac{N_{op}(300)+1}{N_{op}(T)+1} \lambda_{op} \quad (46)$$

$$\lambda_{op,ems}^{fld} = \frac{\hbar\omega_{op} - K_B T}{q \frac{V}{l}} + \frac{N_{op}(300)+1}{N_{op}(T)+1} \lambda_{op} \quad (47)$$

In equations 45, 46 and 47, $N_{op}(300)$ is the value of phonon occupation function at 300 K. K_B in equation 47 is the Boltzmann constant. Carrier scattering path due to optical emission under the influence of electric field ($\lambda_{op,ems}^{fld}$) depends on both the electric field (V/l) and temperature (T). The effective mean free path can now be calculated by Matthiessen's rule as follows,

$$\frac{1}{\lambda_{op,ems}} = \frac{1}{\lambda_{op,ems}^{abs}} + \frac{1}{\lambda_{op,ems}^{fld}} \quad (48)$$

$$\frac{1}{\lambda_{eff}} = \frac{1}{\lambda_{ac}} + \frac{1}{\lambda_{op,ems}} + \frac{1}{\lambda_{op,abs}} \quad (49)$$

Assuming SWCNT as a good conductor and considering only one-dimensional flow we can deduce the current density from equation 40 which is given by,

$$\hat{j} = \frac{e^2 n_0}{m} (1 - \alpha) \frac{1}{\frac{v_F}{\lambda_{eff}} + i\omega} \bar{\varepsilon} \quad (50)$$

where ω is the angular frequency. The current density equation describing the frequency dependent conductivity of the SWCNTs, $\sigma(\omega)$ is expressed by,

$$\sigma(\omega) = \frac{\hat{j}}{\bar{\varepsilon}} = \frac{e^2 n_0}{m} (1 - \alpha) \frac{1}{\frac{v_F}{\lambda_{eff}} + i\omega} \quad (51)$$

$\sigma(\omega)$ is also called as dynamic conductivity of SWCNT. For metallic CNT, semi-classical axial conductivity is given by,

$$\tilde{\sigma}_{zz} = \frac{2e^2 v_F}{\pi^2 \hbar r} \frac{1}{v + i\omega} \quad (52)$$

Combining equations 50 and 51, we obtain,

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$$\frac{n_o}{m} = \frac{2v_F}{\pi^2 \hbar r} \frac{1}{1 - \alpha} \quad (53)$$

where r is the radius of SWCNT. Equation 51 relates dynamic conductivity with the semi-classical conductivity. We have assumed that SWCNT is metallic and placed above a perfectly conducting plane and also assumed that quasi-TEM (transverse electromagnetic) electromagnetic wave is propagating through the SWCNT. The electric field can be expressed as,

$$\varepsilon_z = RI + L_K \frac{\partial I}{\partial t} + \frac{1}{C_Q} \frac{\partial q}{\partial z} \quad (54)$$

where R is the resistance in per unit length, L_K is kinetic inductance in per unit length and C_Q is quantum capacitance in per unit length. The SWCNT interconnect can then be better explained as a transmission line shown in figure 45 where its parameters are described by following equations,

$$L_k = \frac{\pi \hbar}{4e^2 v_F} \quad (55)$$

$$C_Q = \frac{1}{L_K u_e^2} \quad (56)$$

$$C_E = \frac{2\pi\epsilon}{\ln \frac{h}{2r}} \quad (57)$$

$$R = f(\lambda_{eff}) = \frac{R_o}{4} \frac{1}{\lambda_{eff}} \quad (58)$$

$$L_M = \frac{\mu}{2\pi} \ln\left(\frac{h}{2r}\right) \quad (59)$$

In equation 59, h is the height of SWCNT over the perfectly conducting plane and R_0 is quantum resistance taken as 12.906 k Ω and L_M is described by the equation 59 as the magnetic inductance.

In thermal modeling of SWCNT interconnect material, $R(V, D)$ is the voltage (V) and diameter (D) dependent critical parameter which directly depends on the effective mean free path (λ_{eff}). Increase in temperature of interconnect triggers various scattering processes which result in increase of the resistance. This increased resistance limits the current density and eventually limits heat generation. Consequently, an iterative solution is needed to find out the actual converged value for resistance instead of using a direct equation.

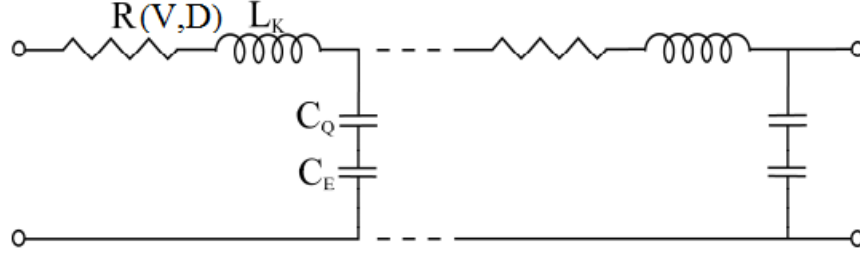


Figure 45 Transmission line model of SWCNT interconnect

3.4.3 Results and Discussion

Temperature profiles along the SWCNT length can be numerically solved from steady state heat equation given by Carslaw and Jaeger,

$$A\nabla(\kappa\nabla T) + p - g(T - T') = 0 \quad (60)$$

where κ is the heat conductivity, A is the Cross sectional area ($\pi \times \text{Diameter} \times \text{Thickness}$), T' is ambient temperature, g is thermal conductivity of the substrate and p is heating source power. In calculation, the terminal temperatures of SWCNT are assumed to be at 350 K which is the normal operating temperature of a typical bulk semiconductor. Therefore, in equation 60, $T' = 350$ K and $g = 0.15 \text{ Wm}^{-1} \text{ K}^{-1}$, have been used. The standard feature size of the CNT has been used so that results can be compared with the findings of other reported work. CNT diameter, D has been taken as 1 nm which is a typical value. Resistance of SWCNT at different biasing voltages and lengths has been calculated by numerically solving equation 60. Since, thermal conductivity (κ) is almost constant within 350 K to 800 K, we have taken thermal conductivity constant at a particular bias voltage. The steps in calculation of resistance are described as follows assuming ambient temperature remains constant as that of the CNT across its length.

1. Consider differential length of CNT and calculate mean free path as well as differential resistance for differential element using equations 49 and 58. Estimate total resistance of SWCNT by summing all differential resistances.
2. Calculate current from equation $I = V/(R + R_c)$, where R_c is the contact resistance 30 K Ω .
3. Calculate $I^2 R$ per unit length for heat generation and then use equation 60 to get temperature profile over the CNT length.
4. Use current temperature profile as the initial temperature for next iteration. Repeat steps 1 to 4 until convergence is obtained.

Figure 46 shows the temperature profile over the length of SWCNT of 2 μm length. At different bias voltages, the temperature profile varies over the length. At biasing voltage above 3 V, the temperature reaches close to the breakdown temperature of 873 K. From figure 46, it can be inferred that biasing voltage less than 4 V is not sufficient enough for causing the breakdown of SWCNT. It is to be mentioned that for low biasing, the iteration requires less than 5 iterations to converge. On the other hand, high bias voltage more than 4 V, calculation takes more iteration to converge.

Figure 47 shows power dissipation versus bias voltage. For 4V biasing voltage, Joule heating power is close to 0.13 mW. As a matter of fact, at a certain bias voltage enough heat will be produced that will be sufficient for inducing breakdown in SWCNT at the mid-point. Higher biasing voltage increases optical phonon emission induced by the higher electric field. According to the equation 47, electron scattering length $\lambda_{op,ems}^{fld}$ decreases with increase in bias voltage which contributes to decrease in effective mean free path (λ_{eff}). The total resistance increases with decreasing effective scattering length. This increase in resistance contributes to increase in Joule heating.

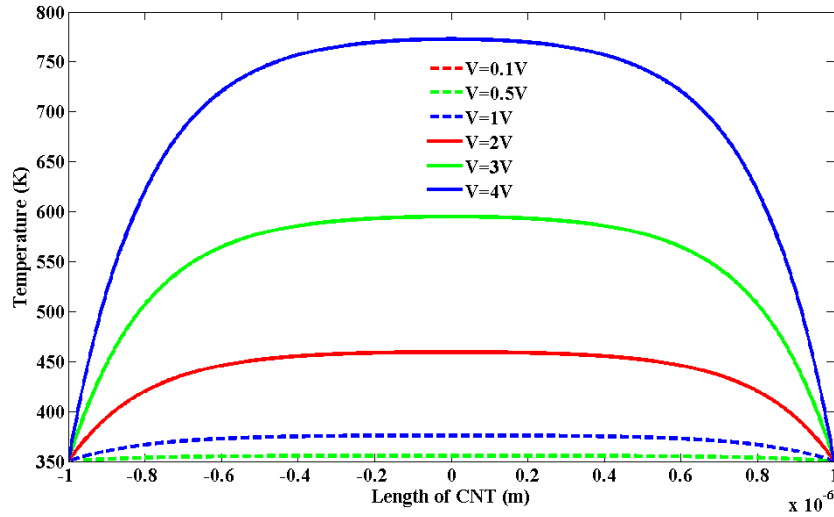


Figure 46 Temperature profile of SWCNT of 2 μm length

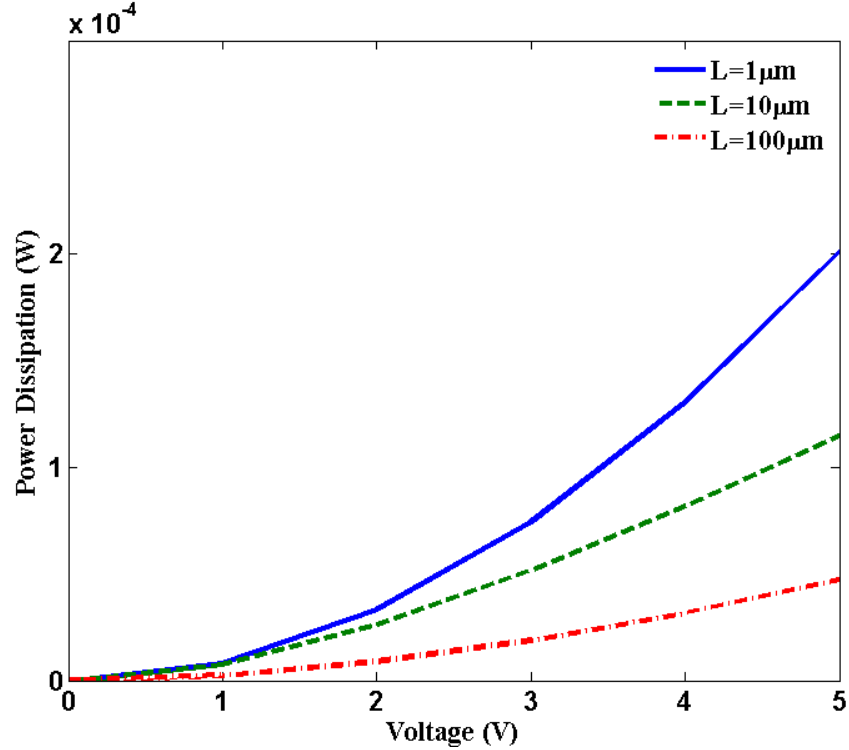


Figure 47 Power dissipation due to Joule heating along the SWCNT length

We have calculated kinetic inductance, $L_K = 3.6 \text{ nH}/\mu\text{m}$, quantum capacitance, $C_Q = 90 \text{ aF}/\mu\text{m}$ and electrostatic capacitance $C_E = 70 \text{ aF}/\mu\text{m}$ of SWCNT transmission line to study S-parameters. Typically, a SWCNT diameter is $\sim 1 \text{ nm}$ and oxide thickness over which SWCNT is deposited is $\sim 100 \text{ \AA}$. The calculated value of $L_M \sim 1 \text{ pH}/\mu\text{m}$ which is very small compared to the value of L_K . The calculated kinetic inductance is consistent with the value calculated for metallic CNTs. It is apparent from equations 55-59 that inductance and capacitance are constant for a specific SWCNT with a given length and diameter. On the other hand, resistance of SWCNT interconnect is a function of bias voltage, SWCNT diameter, length, and temperature which influences scattering parameters. Scattering Parameter S_{11} is the ratio of power reflected from the transmission line to the incident power. Scattering parameter S_{12} is the ratio of power transmitted through the transmission line to the incident power. Two port network parameters S_{11} and S_{12} have been calculated considering lumped elements and normalized by 50 ohm impedance. Although transmission line is a distributed device, we have used lumped element model to calculate S-parameters for the sake of efficient computation. Figures 48 and 49 show plots of S_{11} and S_{12} parameters of SWCNT at 0.1 V bias voltage. At higher frequencies inductive and capacitive terms dominate over the resistive term which results in an oscillatory behavior of S-parameters as observed in figures 48 and 49. Figure 48 for the S_{11} parameter exhibits an oscillatory behavior for $100 \mu\text{m}$ long interconnect above 10 GHz in the frequency range studied. Figure 49 for the S_{12} parameter shows an oscillatory behavior for both $10 \mu\text{m}$ and $100 \mu\text{m}$ long interconnects above 70 GHz and 7 GHz , respectively. However, the short interconnect of $1 \mu\text{m}$ length does not show any oscillatory behavior for S_{11} and S_{12} parameters.

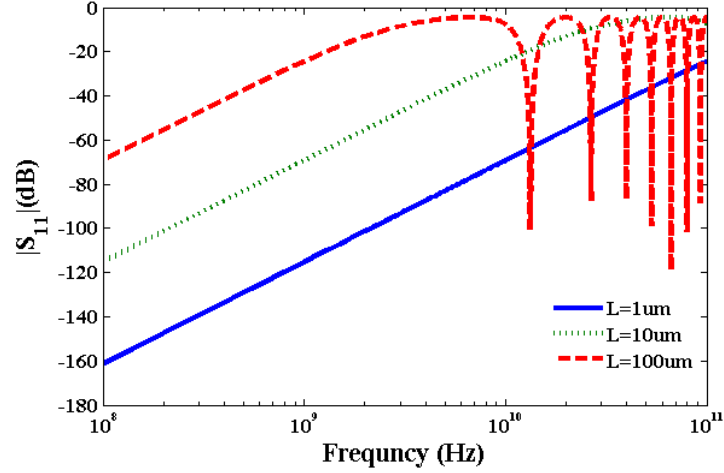


Figure 48 Plot of S_{11} parameter of SWCNT interconnects at 0.1 V bias voltage

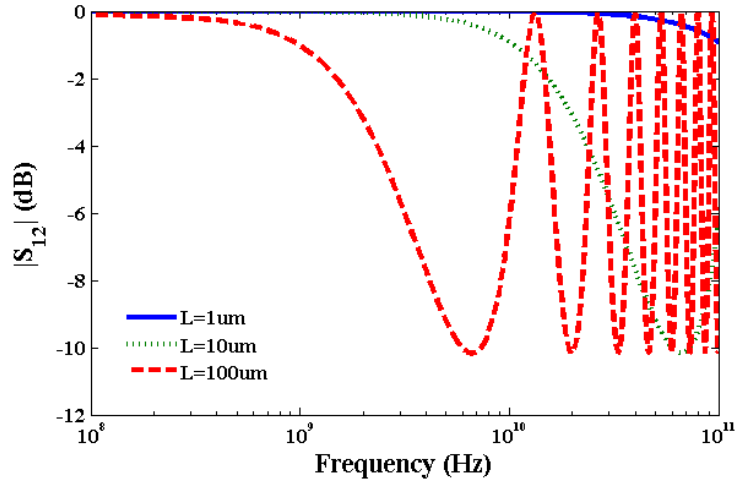


Figure 49 Plot of S_{12} parameter of SWCNT interconnects at 0.1 V bias voltage

Table 7 summarizes the comparison of results with that we have reported in our work without considering the Joule heating and with the Joule heating induced scattering with this current model. We have considered the frequency band in which value of S_{12} parameter is within -3dB of its maximum value at 0.1 V. It is noticeable from table 7 that the bandwidth reduces considering Joule heating due to scattering in comparison to the bandwidth without Joule heating. The frequency band width for a interconnect decreases considering Joule heating induced scattering and increased resistance.

Table 7 S_{12} parameters of SWCNT

Length of SWCNT (μm)	Band Width (GHz) without Scattering	Band Width (GHz) with Scattering
1	1000	120
10	110	11
100	30	1.0

Figure 50 shows resistance variation with the applied current for short local and global interconnects lengths. It is observed that breakdown in SWCNT occurs due to Joule heating which results in an infinite increase in resistance. This theoretical observation agrees with the experimental observation. Figure 51 shows the dependence of S_{12} on bias voltages and shows an increase in S_{12} with increased bias voltage.

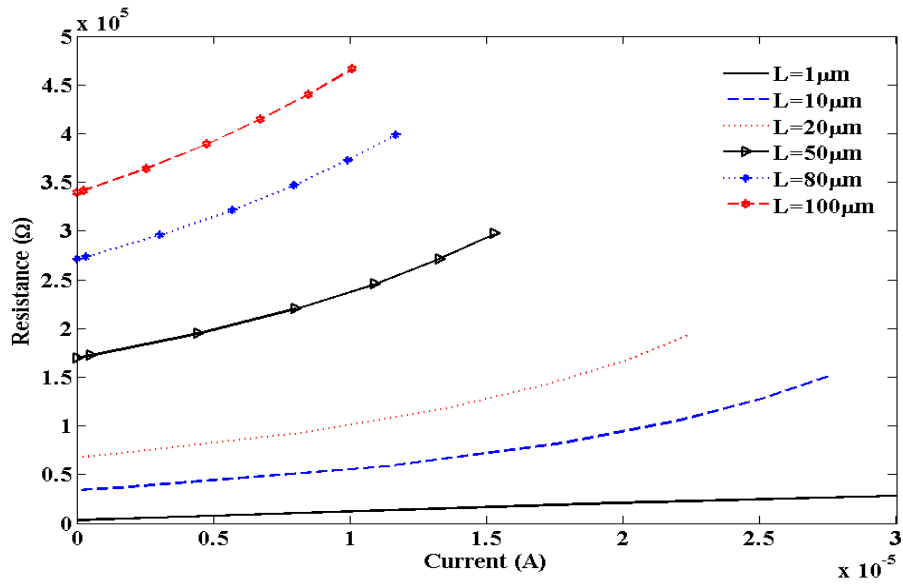


Figure 50 Plot of SWCNT resistance *versus* current

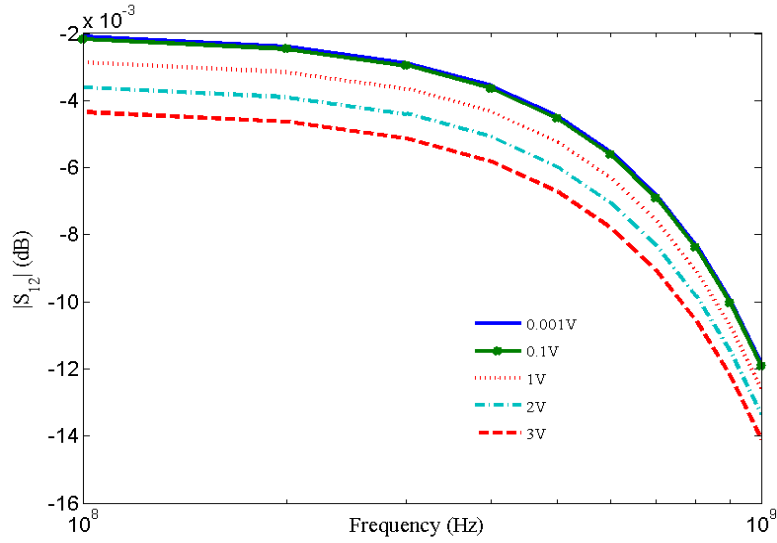


Figure 51 S_{12} parameter of SWCNT interconnects at different bias voltages

3.4.4 Conclusions

In this work, we have incorporated Joule heating induced phenomenon in 1D fluid model of CNT interconnects. We have studied scattering parameters of SWCNT for short, local and global interconnect lengths with different biasing voltages. We have observed that the bias voltage does not greatly affect the scattering parameters; on the other hand it significantly influences Joule heating. The breakdown shown in resistance versus current is clearly notable. The presented thermal model is very useful in experimental studies related to CNT integrated in nm- and sub-nm CMOS technology.

3.5 PART II GRAPHENE-BASED ELECTRONICS

3.5.1 Introduction

The Moore's law of MOSFET scaling is approaching to its near end. The International Technology Roadmap for Semiconductors (ITRS) has listed several non-classical devices to explore future replacement of silicon-based MOSFETs. In search of novel switching devices based on two- and three-dimensional materials, two-dimensional materials have opened up opportunities for novel device structures in emerging post-CMOS technology such as the one based on quantum mechanical tunneling. In particular, tunnel field effect transistor based on two-dimensional graphene has shown potential to operate at low voltage with a low subthreshold slope (SS) compared to 60mV/decade in conventional MOSFETs. Tunneling in graphene transistors has been studied from lateral band-to-band tunneling and vertical tunneling through the thin insulating film. In contrast to band-to-band tunneling in graphene FET, vertical tunneling through the thin insulating film in graphene heterostructures has been studied experimentally and large ON/OFF current ratio of between 10^4 to 10^6 has been obtained. Negative differential resistance in graphene resonant tunneling transistors has also been reported experimentally. A single layer graphene does not possess any band gap, however, quantum confined graphene nanoribbon (GNR) shows an observable band gap.

In addition to ballistic transport in GNR FET, band-to-band tunneling in GNR tunnel FET has been studied by numerical simulations for graphene homo-junctions, hetero-junctions, single and bilayers and dissipative transport through rough edges for the understanding of current transport. Majority of these numerical simulations are obtained by solving 3D Poisson's equation coupled with Schrodinger's equation for a nearest neighbor tight binding (TB) Hamiltonian for a finite width and specific edge type GNR. Since classical drift-diffusion model of current transport becomes inappropriate for such a quantum confined system where the mean free path of a carrier dominates over the scattering, a fully quantum transport model is necessary to predict the operation of such device accurately in multiscale modeling framework. Nevertheless, a well described semi-classical analytical model is important for better understanding and to bridge the gap between experimental data and numerical simulations. A semi-classical analytical model has been reported in the work of Zhang *et al.*. However, the model is neither validated from numerical simulations nor experiments. In this work, current transport in a p-i-n n-type armchair GNR (a-GNR) tunnel field effect transistor (TFET) of 20 nm channel length and 4.9 nm channel width is studied from both analytical and numerical methods. Following the device structure in the work of Zhang et al., this work considers a single gate a-GNR TFET. Two separate current transport models are derived analytically from semi-classical and semi-quantum modeling approaches. Non-equilibrium Green Function (NEGF) based numerical simulation study is also carried out using the open source quantum transport simulation tool, NanoTCAD ViDES. Results obtained from these two methods are compared with the numerical simulation to establish analytical models. Furthermore, a-GNR TFET's performance is studied for varying GNR width using semi-classical, semi-quantum and NEGF simulation based current transport models. Finally, applicability of both analytical (semi-quantum and semi-classical) and numerical models are demonstrated through the computation of voltage transfer characteristic of a complementary a-GNR TFET inverter for digital circuit design.

Graphene nanoribbon (GNR) has two types depending on their edges, zigzag nanoribbon and armchair nanoribbon. Localized edge states at the Fermi level are observed in zigzag edge nanoribbon whereas such edge states are absent in armchair edge nanoribbons. These localized states are important as these infer to localized wave functions at the GNR edges and contribute to antibonding properties of GNR and electronic structure. In this work, armchair GNR is considered as the channel material for the tunnel field effect transistor.

Electrical properties of armchair GNR (a-GNR) is strongly dependent on the number of atoms along its width. Figure 52 shows top view of an armchair GNR drawn using NanoTCAD ViDES where its width varies along the Y direction and length along Z direction. The variable N is an integer. The notation of chirality for a-GNR is expressed as $(n, 0)$ where n is the number of carbon atoms on each ring of unrolled nanotube. Generally such a nanoribbon are termed as $p=2n$ a-GNR in literature where 'p' is defined in terms of any of the configurations from $3N$, $3N+1$ or $3N+2$ along the GNR width. Therefore, a $(7, 0)$ chirality has 14 carbon atoms along its width which is a $3N+2$ configuration not $3N+1$. Whereas $(8, 0)$ a-GNR has 16 carbon atoms which is a $3N+1$ configuration not $3N+2$.

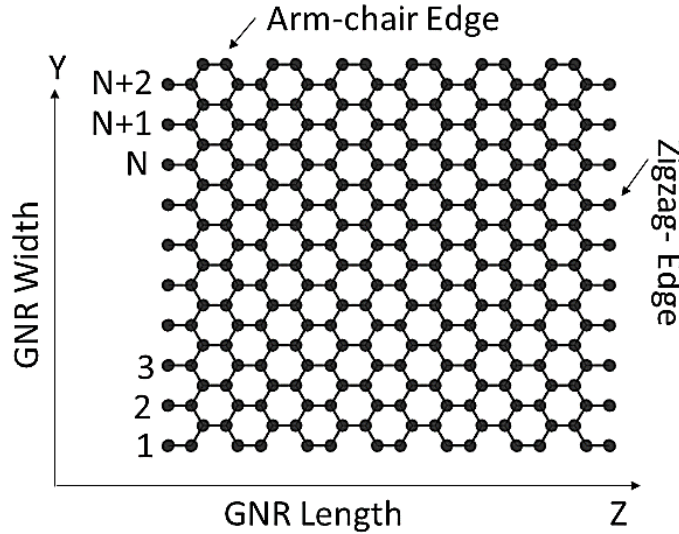


Figure 52 Armchair graphene nanoribbon (a-GNR)

Energy band gap of GNR, both armchair and zigzag, differs depending on the method of calculation. Electronic structure of GNR is modeled traditionally by the simple TB approximation based on π -bonded p_z -orbital electrons or usually studied by Dirac equation of massless particle considering effective speed of light ($\sim 10^6$ m/s). Such assumptions lead to conclude armchair GNR to be either metallic ($3N+2$ configuration) or semiconducting ($3N$ and $3N+1$ configuration). Moreover zigzag GNR with edge states on both sides of ribbon is metallic regardless of its width if computed by the TB approximation. Results obtained by TB approximation considering nearest neighbor hopping integral of 2.7eV show that armchair GNR is metallic for $p=3N+2$ and semiconducting for both $p=3N$ and $p=3N+1$ configurations. Basically the hierarchy of energy band gap is maintained as $\Delta_{3N} > \Delta_{3N+1} > \Delta_{3N+2} (=0 \text{ eV})$, Δ being the energy gap, for all values of N.

On the other hand, first principle calculation using self-consistent pseudopotential method by local (spin) density approximation (L(S)DA), however, shows that there are no metallic a-GNR. The energy gap as a function of width is now grouped in a family of energy gaps and maintains the hierarchy of $\Delta_{3N+1} > \Delta_{3N} > \Delta_{3N+2}$ ($\neq 0$ eV). Such energy gap originates from the quantum confinement and crucial role of edge states and changes with a-GNR width. The Hamiltonian used in this work for estimating a-GNR band gap is adopted for which it always estimates nonzero and direct band gap as opposed to simple TB scheme. Moreover, first principle many electrons Green's function approach within the GW approximation (single particle Green's function G and the screened coulomb interaction W) provides quasi-particle energy gap with additional self-energy correction for both armchair and zigzag GNRs.

Recently, it has been shown that proper consideration of higher energy levels in addition to p_z - orbitals in TB scheme gives more accurate description of the GNR band structure. It is shown that within the TB method $3N+2$ a-GNRs are not really metallic if higher energy levels such as 'd' orbitals are included. This is in agreement with the electronic structure obtained from rigorous first principle based calculations.

The a-GNR of (20, 0) chirality is considered in this work which corresponds to 4.9 nm width and 0.289 eV energy band gap. Both the GNR width and band gap are obtained from NanoTCAD ViDES. Figures 53(a) and 53(b) show the schematic of a single gate TFET with 30 nm long a-GNR on SiO₂ substrate for p-type and n-type, respectively with appropriate biases. Channel length is 20 nm with a 5 nm extension of source and drain at right and left ends. Channel is intrinsic. Source and drain are assumed as n- and p- type doped for p-type and p- and n- type doped for n-type a-GNR TFET, respectively. Chemical doping or electrostatic doping either can be used for doping of GNR.

In electrostatic doping, a positive and negative gate voltage generates n- and p- type graphene, respectively. Moreover, ion doping in graphene sheets can reach electron and hole density around $10^{14}/\text{cm}^2$. Traditionally boron (B) and nitrogen (N) are treated as natural candidates for doping graphene due to same atomic size as in carbon. An n-type doping of GNR can be obtained through electrochemical reaction with NH₃. Such a doping forms C-N bonds at GNR edges. Though the method provides high ON/OFF current ratio of $\sim 10^5$, mobility degrades in n-type GNR FET compared to in pristine GNR FET. One problem associated with it is that N-doped graphene (NG) can be both n- and p-type based on bonding nature of N atoms. Recently, it has been studied experimentally that chemically functionalized array of GNR with 4-nitrobenzenediazonium (4-NBD) and diethylene triamine (DETA) molecules can provide doping of GNR arrays to p- and n-type, respectively. In both cases, due to presence of a large quantity of edges, higher doping effect is observed in GNRs than that in pristine graphene sheets. Since performance of GNR TFET (Fig. 53) is largely dependent on electric field at an abrupt p-n tunnel junction, choosing a suitable doping method for n- and p- type GNR is a critical step in emerging device development.

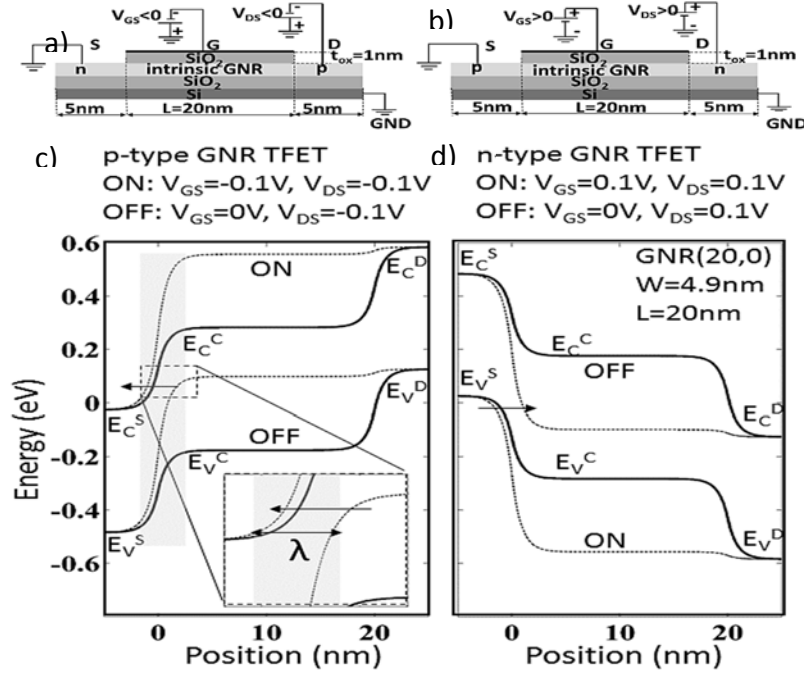


Figure 53 Schematic of a-GNR TFET.

Figure 53(a) Vertical cross section of p-type a-GNR TFET with 1 nm SiO₂ top gate dielectric. Channel length is 20 nm with 5 nm of source and drain extension making the total length of GNR 30 nm, (b) n-type a-GNR TFET, (c) energy band diagram of n-i-p GNR TFET (p-type GNR TFET where both V_{GS} and V_{DS} are ‘-’ ve) and (d) energy band diagram of p-i-n GNR TFET (n-type GNR TFET where both V_{GS} and V_{DS} are ‘+’ ve). Inset: Enlarged view of potential variation.

In figures 53(a) and 53(b), a-GNR is placed on top of SiO₂ substrate. Since single layer graphene is not grown directly on SiO₂ in conventional CVD methods, different methods of either transferring graphene from other metallic substrate such as Cu or Ni or liquid phase exfoliation can be considered. For nanoscale a-GNR of 4.9 width and 20 nm length, lithographically patterned GNR is highly desirable. Silicon dioxide of 1 nm is considered as a top gate oxide. Length of gate dielectric is 20 nm as shown in both figures 53(a) and 53(b). Cr/Au or Ti/Cu contacts are typically used.

By solving 3D Poisson’s equation coupled with 1D Schrodinger’s equation within the NEGF formalism, three-dimensional potential is obtained for a-GNR TFET in all three (X, Y and Z) spatial directions. Corresponding energy band diagrams along the channel are plotted from the channel component (along Z direction) of this potential. Figures 53(c) and 53(d) show the energy band diagram during an off/on condition for n-i-p (p-type) and p-i-n (n-type) TFET, respectively. E_C^S, E_C^C and E_C^D are source, channel and drain conduction bands, respectively, whereas E_V^S, E_V^C and E_V^D are the source, channel and drain valence bands, respectively. The solid and dash lines show OFF and ON states of TFET, respectively. Note that for both types of transistors, OFF state is defined for |V_{DS}| = 0.1 V and |V_{GS}| = 0 V and ON state is defined for |V_{DS}| = 0.1 V and |V_{GS}| = 0.1 V. Throughout this work positive bias of V_{GS} and V_{DS} is considered assuming n-type a-GNR TFET.

Semiconducting a-GNR (20, 0) has a band gap of 0.289eV for its corresponding 4.9nm width. Junction electric field of 3.85×10^6 V/cm is taken into account which is identical with the estimated electric field in the work of Zhang et al. For the p-i-n n-type a-GNR TFET, source and drain are assumed to be p- and n-type where Fermi levels are assumed to coincide with the valence band and conduction bands, respectively.

In thermal equilibrium, Fermi levels in source, channel and drain regions are aligned together. During OFF state there is a difference of $|V_{DS}|$ between E_C^S and E_V^D in p-type TFET and E_V^S and E_C^D in n-type TFET. However, source and channel Fermi levels remain aligned together. Therefore, no tunneling of carriers occurs through source-channel tunnel junction. Further, for $V_{GS} > 0$ (in n-type TFET) and $V_{GS} < 0$ (in p-type TFET), a tunneling window opens and initiates band-to-band tunneling. Direction of arrows shows flow of carriers due to tunneling between source and channel. GNR TFET is less sensitive to channel mobility since band-to-band tunneling dominates over the scattering in channel. Both source and channel are of same material assuming momentum conservation in both conduction and valence bands. The inset and the shaded area in figure 53(c) show the relevant length scale for potential variation (λ) which is usually dependent on the device geometry. For 1D geometry of a-GNR, λ is determined from $\lambda = \sqrt{(\epsilon_{GNR} / \epsilon_{ox}) t_{GNR} t_{ox}}$ where ϵ_{GNR} and ϵ_{ox} are the GNR and oxide dielectric constants, respectively, and $t_{GNR} = 0.35$ nm is the thickness of the GNR. In this work, we consider λ to be significantly lower than the channel length L . For $L \gg \lambda$, it has been found that the drain induced barrier lowering (DIBL) is significantly suppressed thereby yielding an ideal turn-off characteristic.

3.5.2 Current Transport Models

Following three types of current transport models are presented and compared: (a) semi-classical analytical model, (b) semi-quantum analytical model and (c) NEGF-based numerical model.

Figure 54 shows output characteristic (I_D - V_{DS}) of n-type a-GNR TFET using the three current transport models studied in this work for different V_{GS} . The semi-classical analytical model shows good agreement with the results obtained from the numerical simulation, however, the semi-quantum model differs largely.

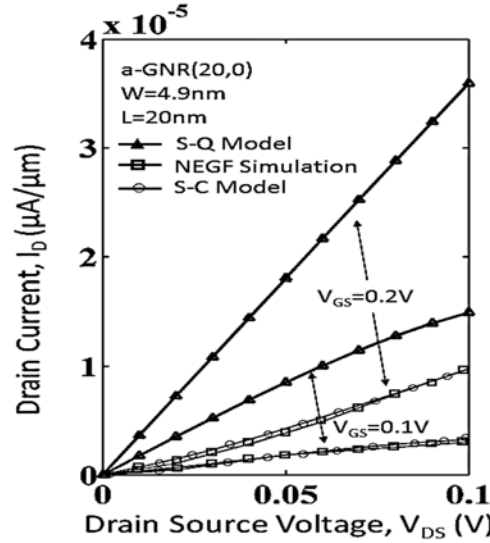


Figure 54 I_D - V_{DS} characteristic of n-type a-GNR TFET for semi-classical analytical model, semi-quantum analytical model and NEGF simulation for $V_{GS}=0.1V$ and $V_{GS}=0.2V$

Figure 55(a) shows schematic of a complementary a-GNR TFET inverter for operation at different supply voltages and is similar to CMOS inverter in design and operation. Characteristics of a-GNR TFET inverter is plotted from all three current transport models. At input logic level “1” (either 0.1V or 0.2V), n-type a-GNR TFET turns ON, p-type a-GNR TFET is OFF and output gives logic “0”. Similarly when input is at logic “0” (0V), p-type a-GNR TFET turns ON and n-type a-GNR TFET is OFF, output is at logic “1” (either 0.1V or 0.2V for the case in figure 55(b)). Figure 55(b) shows plot of voltage transfer characteristics (VTC) of the complementary a-GNR TFET based inverter of figure 55(a) for a-GNR for (20,0) chirality and $V_{DD}=0.1V$ and 0.2V supply voltages.

Following the transfer characteristics obtained for all three current transport models, VTC of a-GNR TFET inverter also shows good agreement between semi-classical analytical model and NEGF simulation. However, semi-quantum analytical model differs from both of these models in this case as well. A decrease in the logic “1” is observed due to inherent leakage current at OFF state for both transistors. However, sharp transition between ON to OFF state is observed at reduced supply voltage. The VTC shown in figure 55(b) confirms the reliable use of semi-classical analytical model for digital circuit simulation with a good agreement with numerical simulation.

By comparing the semi-classical analytical model with the numerical simulation it is evident that the semi-classical analytical model derived in this work can predict near similar performance of a-GNR TFET for different figure of merits. However, semi-quantum analytical model differs from simulation due to inherent limitation in calculation and hence it is not yet reliable in its current form. Therefore, we conclude the semi-classical analytical current transport model as a powerful tool for circuit simulation for digital circuit design.

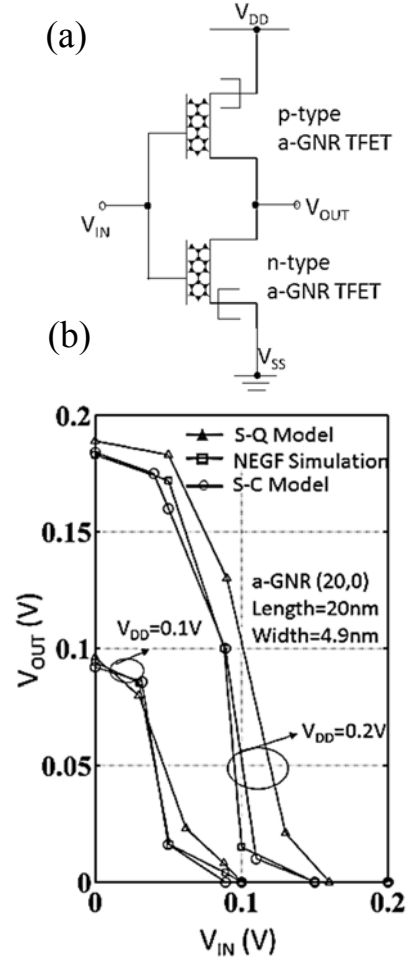


Figure 55 (a) A complementary a-GNR TFET inverter circuit and (b) voltage transfer characteristic of a-GNR TFET inverter for different supply voltages

3.5.3 Conclusion

In this work, semi-classical and semi-quantum current transport models of n-type a-GNR TFET are studied and compared with numerical simulations using NEGF formalism. The semi-classical analytical model closely agrees with numerical simulation whereas significant difference between semi-quantum model and NEGF simulation is observed. Performance of n-type a-GNR TFET is also studied for a-GNR width variation. The semi-classical analytical current transport model of n-type a-GNR TFET can be applied to p-type a-GNR TFETs (n-i-p structure) with opposite voltage polarities. Promise of a-GNR TFET for digital logic application as a TFET inverter is studied by all three current transport models. Characteristics sharp transition from ON to OFF condition is observed for lower supply voltage.

By comparing the semi-classical analytical model with the numerical simulation it is evident that the semi-classical analytical model derived in this work can predict near similar performance of a-

GNR TFET for different figure of merits. However, semi-quantum analytical model differs from simulation due to inherent limitation in calculation and hence it is not yet reliable in its current form. Therefore we conclude the semi-classical analytical current transport model as a powerful tool for circuit simulation for digital circuit design.

3.6 Experimental Research in Graphene for Radiation Hardened Devices

We purchased a BenchTop nanoCVD-8G System from Moorfield, Inc. UK and installed in our Electronics Materials Devices Research Laboratory of Electrical Engineering. We tested the atomic layer deposition of graphene over copper and nickel films and verified the deposited monolayer graphene film from Raman Spectroscopy. Figure 56 shows the demonstration of graphene deposition by CVD technique and equipment by one of my doctoral students working on graphene research for Radiation-hardened devices and experimental results from Raman Spectrometer are shown in figure 57.



Figure 56 Demonstration of graphene deposition by CVD technique

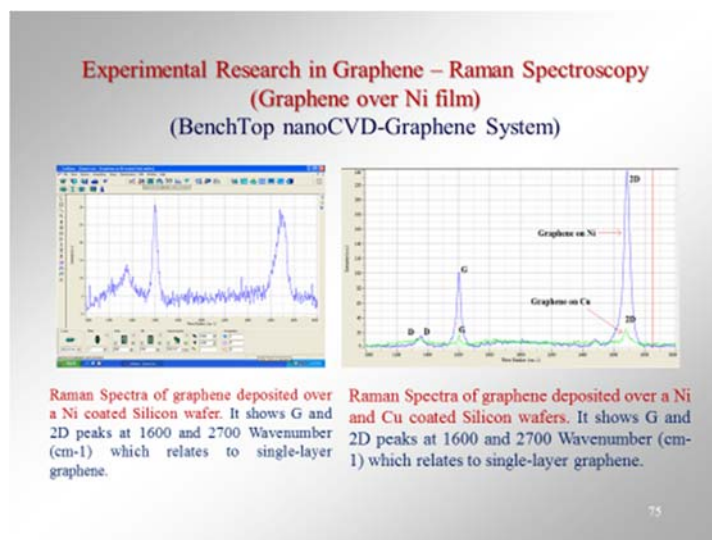


Figure 57 Raman spectra of graphene deposited on Ni and Cu coated silicon substrates

Dr. Ashok Srivastava made a planned visit to US AFRL, KAFB from Nov. 5-7, 2014 and met Dr. Ashwani Sharma, Mr. Clay Mayberry and presented the review of the work done since the beginning of the contract research before the distinguished scientists of the branch. He also had an opportunity to visit research facilities of laboratory for on-going collaboration. Visit was also arranged for UNM-AFRL COSMIAC Center and UNM Center for High Technology Materials. Dr. Srivastava gave graphene deposited copper and nickel samples to Mr. Clay Mayberry and Dr. Sharma for Co-60 radiation exposure studies. The visit was very productive and is expected to continue in the direction of both theoretical and experimental research in the field of reduced dimension materials of direct interest to AFRL.

4. RECOMMENDATIONS

Following are the few specific recommendations based on the work conducted as a part of the concluded grant.

- Theoretical and experimental studies on radiation-hard graphene electronics
- Studies on non-graphene types materials-based transistors for integrated circuit design
- Photoconduction and photo-voltaic studies on graphene and graphene based devices
- Studies on hybrid-materials type structure such as copper-graphene for replacement of copper in VLSI interconnects

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

Acronym/ Abbreviation	Description
1D	one-dimensional
2D	two-dimensional
AMS	Analog Mixed-Signal
BTE	Boltzman Transport Equation
CMOS	complementary metal oxide semiconductor
CNT	carbon nanotube
CO	Carbon Monoxide
Cu	Copper
CVD	chemical vapor deposition
DETA	Diethylene Triamine
DIBL	Drain Induced Barrier Lowering
DNA	Deoxyribonucleic Acid
FET	field-effect transistor
G	graphene
GNR	graphene nano ribbon
HiPCO	high pressure carbon monoxide
ITRS	International Technology Road Map for Semiconductors
LC	Inductor Capacitor
L(s)DA	Local spin Density Approximation
MCH	Mercaptohexanol
MoO ₃	Molybdenum Oxide
Mo ₂ C	Molybdenum Carbide
MOSFETS	metal oxide semiconductor field-effect transistor
MWCNT	multi-walled carbon nanotube; multi-wall carbon nanotube
NAND	negative and
NBD	Nitrobenzenediazonium
NEGF	non-equilibrium Green function

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NG	N-doped graphene
PLL	Phase Locked Loop
PVD	physical vapor deposition
RF	radio frequency
SiO ₂	Silicon Dioxide
SOI	silicon on insulator
SRC	Semiconductor Research Corporation
SWCNT	single-walled carbon nanotube; single-wall carbon nanotube
TB	tight-binding
TEM	transverse electromagnetic
TFET	Tunnel Field Effect Transistor
VCO	Voltage Controlled Oscillator
VLSI	very large scale integration
VTC	Voltage Transfer Characteristic

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